LEAKAGE POWER REDUCTION IN CMOS CIRCUITS USING LEAKAGE CONTROL TRANSISTOR TECHNIQUE IN NANOSCALE TECHNOLOGY

Abhishek Sharma¹, Shipra Mishra²
¹M.Tech. Embedded system & VLSI Design NITM, Gwalior M.P. India 474001
²Asst Prof. EC Dept., NITM, Gwalior, M.P. India 474001

Abstract: In this paper, we propose a leakage reduction technique. Because high leakage currents in deep submicron regimes are becoming a major contributor to total power dissipation of CMOS circuits. Sub threshold leakage current plays a very important role in power dissipation. So to reduce the sub threshold leakage current we proposed an adaptive voltage level (AVL) technique. Which optimize the overall voltage across the half subtractor circuit in active mode. In this AVL technique, Two schemes are employed, one is AVLS (adaptive voltage level at supply) in which the supply voltage is reduced and the other is AVLG (adaptive voltage level at ground) in which the ground potential is increased. By applying this technique we have reduced the leakage current from 9.274pa to 5.428. That means this technique the leakage current 41.4% .the circuit is simulated on cadence virtuoso in 45nm CMOS technology. Simulation results revealed that there is a significant reduction in leakage current for this proposed cell with the AVL circuit reducing the supply voltage.

Key words: Low power VLSI, leakage current, half-subtractor, CMOS, AVL technique.

I. INTRODUCTION

As a result of scaling, power dissipation due to leakage currents has increased dramatically and is a major source of concern especially for low power applications. Till now, the dominant leakage mechanism has been due to drain-source sub-threshold current. Assuming this leakage mechanism, a number of techniques have been proposed in literature for reducing the impact of leakage power dissipation such as gated-VDD scheme [1, 2], Dual-Vth SRAM [3] etc. With scaling of channel length, oxide thickness also needs to be scaled to maintain proper operation of MOS transistor. As a result, even though supply voltage has been reduced with new generations of technology, the magnitude of gate leakage current has increased steadily and is likely to become comparable or even larger than the sub-threshold leakage for future CMOS devices [4]. With the perspective that leakage power dissipation in logic circuit would constitute a significant fraction of overall power dissipation, an analysis of leakage currents in a half subtractor has been carried out and techniques for suppressing it are compared. Most of the techniques that have been proposed in the last few years to lower the sub-threshold leakage and gate leakage in logic and combinational circuits use reduced effective supply voltage to circuit during the inactive state. A few change the transistor substrate bias voltages during the inactive state. These techniques are associated with long wake-up latency when circuit changes from inactive state to active state and larger dynamic power dissipation when circuit changes from one state to another state. Low leakage asymmetric cells that reduce sub threshold leakage currents were proposed by N.Azizi etal., [5,6]. These cells exploit the fact that most of the bits stored in caches are zeroes. In this work, a half subtractor is proposed that offers reduced gate and sub threshold leakage currents in caches without significant degradation in the performance. In this work, a conventional half subtractor circuit is basically considered and its leakage components are identified. Of the several techniques that have been proposed to reduce sub threshold leakage in logic circuit [3,7,8], use of a self controllable switch (SVL) [9] which allows full supply voltage to be applied during active mode and reduced supply voltage in
inactive mode appears to be particularly promising for reducing gate leakage currents as well. An SVL can be used either to reduce the supply voltage to the HS circuit or increase the potential of ground node and the two approaches can be combined as well. So, in this work, in order to suppress the leakage further, the proposed HA circuit I combined with adaptive voltage level (AVL) circuit either at the ground node (referred as AVLG) or the supply node (referred as AVLS) is simulated and its leakage characteristics are analyzed. The paper is organized as follows. Section 2 describes the conventional HA circuit and its leakage components. Section 3 describes the proposed HS circuit and its operation. Section 4 describes the AVL Circuit and its effect on leakage reduction. Section 5 gives the simulation results and discussion. Section 6 gives the conclusion.

II. SOURCE OF LEAKAGE POWER

There are four main sources of leakage current in a CMOS transistor (see Figure 1).

1. Reverse-biased junction leakage current ($I_{REV}$)
2. Gate induced drain leakage ($I_{IGIDL}$)
3. Gate direct-tunneling leakage ($I_{G}$)
4. Subthreshold (weak inversion) leakage ($I_{ISUB}$) as described next.

![Diagram of CMOS Transistor](image)

**Junction Leakage**

The *junction leakage* occurs from the source or drain to the substrate through the reverse biased Diodes when a transistor is OFF. A reverse-biased pn junction leakage has two main components: one is minority carrier diffusion/drift near the edge of the depletion region; the other is due to electron-hole pair generation in the depletion region of the reverse-biased junction [7]. For instance, in the case of an inverter with low input voltage, the NMOS is OFF, the PMOS is ON, and the output voltage is high. Subsequently, the drain-to-substrate voltage of the OFF NMOS transistor is equal to the supply voltage. This results in a leakage current from the drain to the substrate through the reverse-biased diode. The magnitude of the diode’s leakage current depends on the area of the drain diffusion and the leakage current density, which is in turn determined by the doping concentration. If both n and p regions are
heavily doped, band-to-band tunneling (BTBT) dominates the pn junction leakage [8]. Junction leakage has a rather high temperature dependency (i.e., as much as 50 – 100 x/100 oC, but it is generally inconsequential except in circuits designed to operate at high temperatures (> 150oC.) Junction reverse-bias leakage components from both the source-drain diodes and the well diodes are generally negligible with respect to the other three leakage components.

**Gate-Induced Drain Leakage**
The *gate induced drain leakage* (GIDL) is caused by high field effect in the drain junction of MOS transistors. For an NMOS transistor with grounded gate and drain potential at VDD, significant band bending in the drain allows electron-hole pair generation through avalanche multiplication and band-to-band tunneling. A deep depletion condition is created since the holes are rapidly swept out to the substrate. At the same time, electrons are collected by the drain, resulting in GIDL current. This leakage mechanism is made worse by high drain to body voltage and high drain to gate voltage. Transistor scaling has led to increasingly steep halo implants, where the substrate doping at the junction interfaces is increased (cf. Figure 1), while the channel doping is low. This is done mainly to control punch-through and drain-induced barrier lowering while having a low impact on the carrier mobility in the channel. The resulting steep doping profile at the drain edge increases band to band tunneling currents there, particularly as VDB is increased. Thinner oxide and higher supply voltage increase GIDL current. As an example, with a VDG=3V and Tox of 4nm, there is roughly a 10 fold increase in the GIDL current when VDB is increased from 0.8V to 2.2V.

As transistor length and supply voltage are scaled down, gate oxide thickness must also be reduced to maintain effective gate control over the channel region. Unfortunately this results in an exponential increase in the gate leakage due to direct tunneling of electrons through the gate oxide [10]. An effective approach to overcome the gate leakage currents while maintaining excellent gate control is to replace the currently-used silicon dioxide gate insulator with high-K dielectric material such as TiO2 and Ta2O5. Use of the high-k dielectric will allow a less aggressive gate dielectric thickness reduction while maintaining the required gate overdrive at low supply voltages [11].

**Subthreshold Leakage**
Subthreshold (or weak inversion) conduction current between source and drain in a MOS transistor occurs when gate voltage is below $V_{th}$ [12]. In the weak inversion, the minority carrier concentration is small, but not zero. Weak inversion typically dominates modern device off-state leakage current due to the low $V_{th}$. The weak inversion current can be expressed as [12], eq.1

$$I_{ds} = \mu_0 C_{ox} \left( \frac{W}{L} \right) (m - 1)(Vt) 2. e^{\frac{V_g - V_{th}}{mV_T}} (1 - e^{-V_{ds}/V_{t}})$$

Where $m = 1 + C_{dm}/C_{ox}$

### III. CONVENTIONAL HALF-SUBTRACTOR CIRCUIT
A conventional HS circuit consists 18T. in which 9T pmos and 9t nmos are used. A half subtractor is a combinational logic circuit that subtracts one bit from another. This circuit has two inputs, the minuend and the subtrahend bits, and two outputs the difference and borrows bits. The truth table shown in TABLE is constructed from the binary arithmetic operations. A practical use of half subtractor is for full in a digital system.
Here we can see that there are two inputs A and B and two outputs O/P1 and O/P2. Table (1) shows the truth table of Half subtractor design. Fig (3) shows the transistor level half subtractor design circuit. We can see, there are total ‘18’ transistors used to implementing the circuit, in which ‘9’ are PMOS transistors and rest of ‘9’ are NMOS transistors.

In conventional half subtractor we calculate the leakage current in ideal model is much leakage. Due to this leakage circuit consume more power and system is heating. To reduce this leakage we proposed a technique.
IV. AN ADAPTIVE VOLTAGE LEVEL (AVL) CONTROL CIRCUIT

An adaptive voltage level control circuit [10] can be used either at the upper end of the cell to reduce supply voltage (AVLS scheme) or at the lower end of the cell to raise the potential of the ground node (AVLG scheme). The impact of these two techniques on leakage currents is described in this section.

Leakage control using AVLG

Figure 4 shows a schematic of a Half subtractor in which AVLG scheme [10] is applied. The switch provides 0 Volt at the ground node during the active mode and a raised ground level (virtual ground) during the inactive mode. An increase in virtual ground voltage reduces the gate-source and gate-drain voltage of transistor M9 and also the gate drain voltage of transistor M10, which results in a sharp reduction in gate leakage currents of these two transistors. There is no improvement in gate leakage currents of transistors M5 and M6. But an additional gate leakage appears in transistor M5 due to decrease in drain voltage of M1. Incorporation of AVL results in another new gate leakage current through NMOS transistor NL1 in the AVL switch. As far as sub threshold leakage currents are concerned, AVLG approach is successful in reducing currents through M3, M2 and M5 as well. Thus AVLG approach is completely successful in reducing all sub threshold leakage currents but it is only partially successful in reducing gate leakage currents.

Leakage control using AVLS

An half subtractor incorporating AVLS scheme is shown in Figure 4. In this scheme, a full supply voltage of VDD is applied to half subtractor in active mode while a reduced supply voltage of VD is applied in inactive mode. Since transistor M3 and M4 is in ON state, the drain voltages of transistors M1, M11, M12 and M15 are also at VD. The gate leakage currents of transistors M1 and M2 get reduced due to the decrease in their gate-source and gate-drain voltages respectively. A decrease in source voltage of transistor M6 results in a decrease in gate leakage through it. The gate leakage through transistor M5 remains unchanged. As far as the subthreshold leakage currents are concerned, they are reduced in transistors M2 and M3 but remain unaltered in M3. in HS are ‘0’s the net reduction in the leakage was 37.6% at 27ºC. At 110ºC, the net reduction of leakage currents was 28.2%. Further, a new...
subthreshold leakage current appears in M6 due to the reduction in drain voltage. This additional subthreshold leakage current through access transistors can be reduced by making the bit lines floating. Hence, this approach is more successful in reducing gate leakage currents than AVLG but still leaves two gate leakage current components unaltered.

**Fig (5). Half subtractor using AVLS technique**

V. SIMULATION RESULTS

A binary half subtractor subtracts two input bits and gives the output in the form difference and borrows. We design a transistors level half subtractor circuit with the help of virtuoso tool box, we give some inputs to the subtractor and got some outputs, we use a adaptive voltage level ground technique to reduce the leakage current and leakage power of the half subtractor circuit at 45 nanometer technology. We find some good results in the form of wave forms as shown in fig (7), the leakage current is reduces to 4 pa and the leakage power is 139pw.

**Fig (6). Waveform of C0**
Fig (8). Waveform C1

Fig (9). Waveform C2
Fig(10). waveform leakage current of conventional half subtractor

Fig(10). waveform leakage current in proposed half subtractor
VI. CONCLUSION

Simulation results demonstrated the reduction in power dissipation by using AVL. The results show a reduction in leakage current and leakage power compared to previously available models. For designing of half subtractor using 45 nanometer technologies reduces power consumption, occupies less area as compared conventional half subtractor CMOS technology. In the proposed half subtractor leakage current reduce from 9.274\(\text{pA}\) to 5.428\(\text{pA}\), it is 90.4\% minimum leakage in compare to conventional half subtractor.

REFERENCES