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A REVIEW OF CARRIER MOBILITY AND DRAIN CURRENT ENHANCEMENT IN STRAINED Si CHANNEL MOSFET

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Abstract— As the time is going on the technology is growing with the devices small in size and better performance. There are several ways to improve performance of very large scale integrated (VLSI) circuits and to meet technology requirements. But one of the emerging trends in VLSI circuit is to use strained Si channel MOSFETs to achieve better performance. In this article we have reviewed various methodologies to induce strain in channel & their effect on physical structure and performance of device.
Keywords—SOI, ϵ-Si, mobility, MOSFET, SiGe.

I. INTRODUCTION

A rapid growth in the study of strained silicon due to its potential ability to improve the performance of very large scale integrated (VLSI) circuits independent of geometric scaling can easily be seen in past several years. The practical benefit of scaling is to reduce physical and economical limits are approached. The substrate [ϵ-Si, silicon-on-insulator (SOI) wafers] is emerging as an important way to continue circuit performance enhancement. MOSFET performance improvements are continuing via ϵ-Si channels which are being embraced in nearly all 90, 65, and 45 nm logic, communication, and consumer technologies. The discovery of strained Si to enhance MOSFET performance originated in the research of growing Si layers on SiGe wafers in the early 1980s, but the physical mechanism for the enhancement can be traced back to the censorious work on distortion potentials by Bardeen and Shockley and experimental measurements of piezoresistance by Smith. Strain improves MOSFET drive currents by basically changing the band structure of the channel and can therefore enhance performance even at energetic scaled channel lengths. Strained Si material has appeared as a best option for developing transistors for the next generation electronics. Strain lifts the degeneracy of the valence and conduction bands which can be used to provide superior transport properties in comparison to bulk Si. Transistors fabricated using ϵ-Si layers have reported larger drive currents ability due to the enhanced electron and hole mobility. Possible applications of strained Si include high-speed products like microprocessors, microcontrollers and low-power circuits in wireless communication [1, 2, 5].

II. STRAINED SILICON FORMATION

Strain in the thin film lattice can be induced due to various reasons, including lattice constant differences, inclusion of atoms of impurities in the interstitials, and thermal processing. However, not all strain in the lattice is constructive and beneficial to the device. There are various number ways to induce strain in the silicon lattice. The key requirement is to make process repeatable, cost effective and compatible with existing manufacturing technology, and able to withstand the thermal cycles. There are various types of strain which can be applied either in one, two or three dimensions, each having its own effect on the physical properties of the material. The two major straining techniques widely studied and used in the industry are biaxial strain and uniaxial strain. Biaxial strain is strain to the lattice in the x-y plane with a negative compressive strain in the z direction. The other type of strain is process–induced strain or uniaxial strain, where the principal strain lies in one direction and other two directions adjust to match. Figure 1 shows the collective summary of different methods of straining techniques [13, 14].

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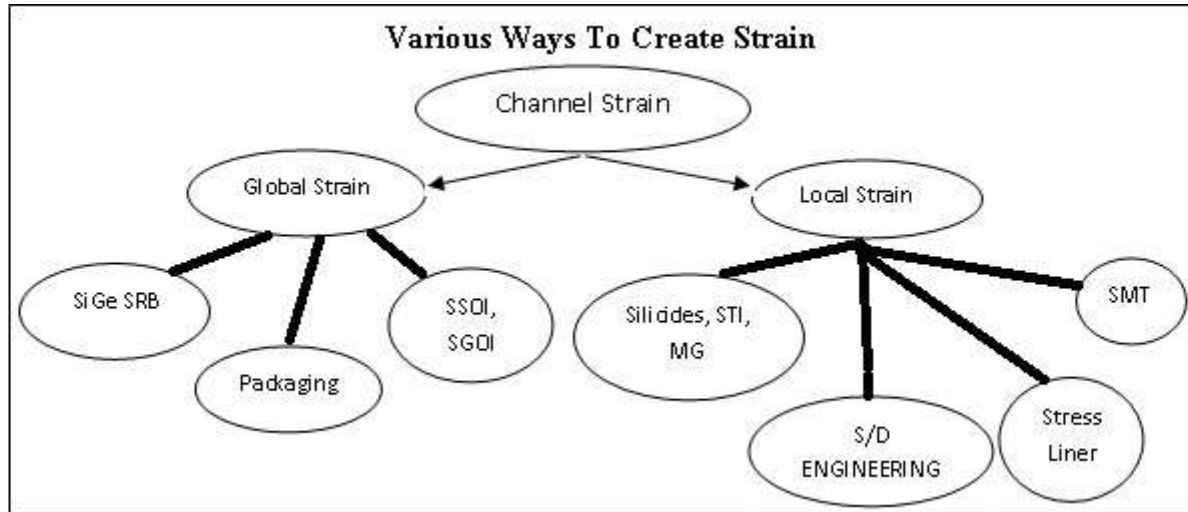

Figure 1. Different Methods of Straining Si Lattice.

A. Uniaxial stress Generation

Uniaxial stress generation process is a widely adopted process in almost all high performance logic technology devices. In uniaxial process-induced strain, the strain is added in the channel layer lower the gate/gate dielectric stack in the (110) plane by introducing a tensile/compressive stressed nitride capping layer on the device structure. A predominant method for depositing an ultra high stress nitride layer is plasma enhanced chemical vapour deposition process along with post deposition treatment at high temperature (~ 650°C) to minimize hydrogen content and maximize stress enhancement. In this process a tensile plasma-enhanced nitride (TPEN) layer is first deposited over the device and then selectively etched over p-MOS leaving a tensile stressed n-MOS, followed by compressive plasma-enhanced nitride (CPEN) layer deposition over p-MOS. Because these stress lines also act as an etch stops for contact etch, this approach is referred to as dual etch stop liners (DESL). This process is mostly used by IBM and AMD with SOI integration. However, this process has a drawback due to dependence on geometry and gate pitch. With stress liners the key is to achieve and maintain conformality of the film without pinching off the top of overlayer film. To accommodate these limitations, the process integration challenge involves the thinning of nitride stress liners without degradation of stress [5].

B. Biaxial Stress Formation

A widely adopted approach to introduce wafer-based stress relies on the fact that the lattice constant of SiGe alloy is slightly larger than pure Si. When a film is pseudomorphically deposited on a substrate, the mismatch strain between the two layers due to difference lattice constant is given by

$$\epsilon_{strain} = (a_{sub} - a_{film})/a_{sub} \quad (1)$$

where a_{sub} and a_{film} are the lattice in substrate and film, respectively. The stress then can finally be computed based on Hooke's law as

$$\sigma_0 = -2\gamma(\nu + 1)/(\nu - 1)\,\epsilon_{strain} \quad (2)$$

where γ is the shear modulus and ν is the Poisson ratio. As there is a 4.2% lattice mismatch between Si and Ge, the strain induced by lattice modifies the band-structure of the SiGe layer and Si layer. Whenever a silicon germanium film is deposited over Si, it is forced to accommodate a film with lower lattice constant; hence the silicon germanium film is under a longitudinal and transverse compressive stress with an out-of-plane tensile component. On other hand, if a Si film is deposited on

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a SiGe film, a biaxial longitudinal and transverse tensile stressed layer is produced with an out-of-plane compressive component [5].

III. PHYSICAL BACKGROUND

Due to the lattice mismatch, a pseudomorphically grown Si layer on a relaxed SiGe buffer experiences a biaxial tensile strain, provided that the layer thickness is below a critical value to prevent strain relaxation. Recently other methods for generating strain in Si have been proposed. Biaxial strain leads to a modification of the conduction band, as shown in Fig. 2. The 6-fold degenerate Δ_6-valleys in Si is being split into 2-fold degenerate Δ_2-valleys (lower in energy) and 4-fold degenerate Δ_4 valleys (higher in energy). The lower in-plane effective mass of electrons in the Δ_2 valleys and the reduction of inter-valley phonon scattering lead to an enhancement of electron mobility [2].

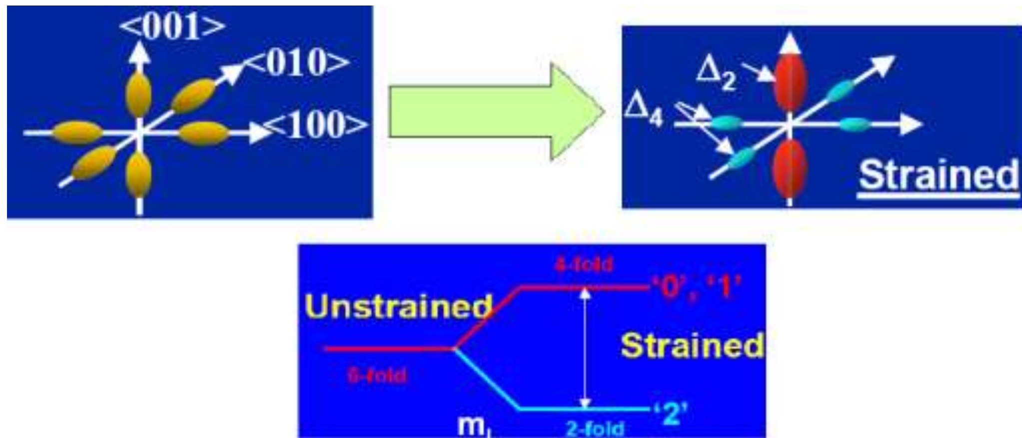

Figure 2. Conduction band splitting in tensile-strained Si (right) compared to unstrained Si (left).

IV. MOBILITY IN RELATED DEVICE

The mobility of carrier in strained Si devices is evaluated as a function of effective electric field (E_{eff}). The decrease in μ_{eff} that takes place as a function of gate voltage V_{GS} in Si inversion layers has been well known for decades and defined as

$$\mu_{eff} = (Leff/Weff)I_{DS}/[C_{OX}(V_{GS} - V_T)V_{GS}] \quad (3)$$

Increasing V_{GS} beyond threshold V_T increases the inversion charge density in the channel Q_{inv} which, by Gauss's law, also increases the electric field perpendicular to the channel (vertical electric field). The electric field at the Si/SiO2 interface is equal to

$$E_{surface} = (Q_b + Q_{inv})/\epsilon_o k_{Si} \quad (4)$$

where Q_b is the charge density in the depletion region, ϵ_o is the vacuum permittivity, and k_{Si} is the relative dielectric constant of Si. After some time the concept of an effective field E_{eff} was introduced as a means to take into account the finite width of the inversion layer W and to quantify the vertical electric field at the average position z_{av} of inversion carriers. E_{eff} is defined as

$$E_{eff} = (Q_b + \eta Q_{inv})/\epsilon_o k_{Si} \quad (5)$$

The value of η used in Eq. (5) was found to be 1/2 for electrons and 1/3 for holes. When plotted as a function of E_{eff} instead of $E_{surface}$, μ_{eff} for electrons and holes falls onto a respective universal curve over a wide range of substrate doping densities (Fig.3).

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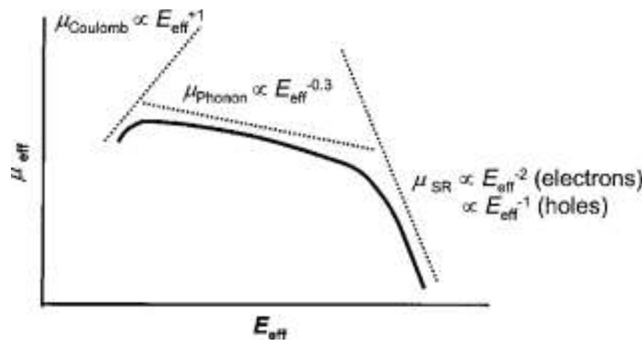

Figure 3. Schematic universal mobility curve for bulk Si MOSFETs[1].

For devices with high substrate doping (e.g., $\geq 10^{18}$ cm^{-3}), E_{eff} near threshold can be very high, and the maximum value of μ_{eff} may be quite low. In this regime of gate voltage, μ_{eff} can lie substantially below the universal curve. As V_{GT} and Q_{inv} increase, Coulomb scattering centres become screened out, and μ_{eff} increases exponentially proportional to E_{eff}^{+1}, eventually rejoining the universal curve. In this regime, acoustic phonon scattering dominates the mobility, and μ_{eff} decreases as $E_{eff}^{-0.3}$. For the highest E_{eff}, both surface-roughness scattering and phonon scattering (at room temperature) are active, and μ_{eff} decays more strongly. While no single power law can be observed at room temperature, at 77 K, μ_{eff} decreases proportional to E_{eff}^{-2} for electrons and E_{eff}^{-1} for holes. The Coulomb-, phonon-, and surface-roughness-scattering limited mobilities are often taken as three separate terms: $\mu_{Coulomb}$, μ_{Ph}, and μ_{SR}, respectively.

It would be advantageous from the perspective of drive current to operate MOSFETs in the higher mobility, low E_{eff} range (i.e., < 0.5 MV/cm), high channel doping density is needed to control V_T in planar-geometry, short channel devices. The high E_{eff} and resulting low μ_{eff} that inversion carriers experience in MOSFETs can be seen as a detrimental and necessary side effect of channel length scaling. Therefore, the usefulness of e-Si lies in its ability to fundamentally alter the band structure in ways that increase μ_{eff} [1, 6].

V. PREVIOUS ANALYSIS

The effect of strain on semiconductor device was first considered in 1950 after that the discovery of strained Si to enhance MOSFET performance originated in 1980. Thereafter many researchers used different methodology to demonstrate their ideas to achieve better performance. The following table.1 to be considering for different methodology has taken and their effects in strained Si MOSFETs.

TABLE 1. COMPARISON OF VARIOUS STUDIES(2, 3, 6, 7, 8, 9, 12)

Author Name	Objectives	Parameters	Results	Remarks
Zhi-Yuan Cheng, Matthew T. Currie and Chris W. Leitz (2001)	To enhance e^- mobility in ϵ-Si n-MOSFET fabricated on SGOI substrate with a high Ge content of 25%.	$G(W_{eff}/L_{eff})$ = 0.138, t_{ox} = 326 nm.	The measured e^- mobility enhancement for ϵ-Si n-MOSFET is significant (1.7 times) when compared to bulk Si.	Large square ring structure n-MOSFETs (L = 200µm, ring Perimeter = 4*250µm) were used to evaluate the e^- mobility as a function of vertical field

Jakub Walczak and Bogdan Majkusiak (2007)	To calculate and compare mobility and drain current of in є-Si MOSFET with relaxed material.	N_{sub} = 2*10^{16} cm^{-3}, 3.1*10^{17}cm^{-3}, 7.7*10^{17}, 2.4*10^{18}, L = 25nm, t_{ox} = 1.6 nm, k_{ox} =7.	Significant mobility and drain current have been obtained, resulting biaxial tensile strain in the channel.	The effective mobility is calculated by combining the phonon scattering, the Coulomb scattering, and - the surface roughness scattering.
S. Dhar, H. Kosina, V. Palankovski, E. Ungersb¨ock, and S. Selberherr (2004)	To develop model describing the anisotropic e^- mobility in є-Si MOSFET.	η = 0.65, λ = 2.0, C^{mid} = 1.12*10^{17} cm^{-3}, $C_{min}{}^{hi}$ = 4.35*10^{19} cm^{-3}	The increase in the in-plane electron mobility is linear, characterized by the piezo resistance coefficients	Changing the shear deformation potential Eu from 9.29eV to 7.3eV gives good agreement for low strains
G. Hadjisavvas, L. Tsetseris, and S. T. Pantelides (November 2007).	To Report first-principle fully quantum-mechanical mobility calculations based on an atomic-scale interface model.	$Si_{1-x}Ge_x$, ΔV = V_{def} – $V_{ref,}$	The seemingly small strain-induced reduction of the scattering potentials has a significant effect on e^- mobilities, for 1% biaxial tensile strain.	Strain-induced enhancement is essentially uniform as a function of electron density.
M. H. Liao, Lingyen Yeh, T. L. Lee, C. W. Liu, and M. S. Liang(April 2008).	To achieve high-performance n-FET by ultrahigh-stress contact-etch-stop-layer stressor and optimal design of device dimensions.	B_{sat}, V_{inj}, r_{sat}, W and L.	when W decreases from 10 μm (low symmetry) to 80 nm (high symmetry) for the L = 55-nm device, both of them are good for the μ_e enhancement	The detailed reason on slight variation of stress along the channel with different gate-width device (10–0.3 μm) is still unclear
Tsung Yi Lu and Tien Sheng Chao(April 2005).	To fabricate a local strained channel nMOSFET by a stress control technique utilizing a stacked a-Si/poly-Si gate and a SiN capping layer.	V_D = 3V, V_G – V_T = 2 V, C_{ox}, G_M, I, t_{ox}.	With the capping SiN-layer, the G_M increases 17% causes 10% increase in I_D; while 29% increase G_M in and 17% increase in I_D can be achieved when using both capping SiN-layer and stacked gate	The thicker the є-Si thickness, the more tensile stress can be induced.
J. Welser, J. L. Hoyt, and J. F. Gibbons(March 1994).	To demonstrate enhanced performance of nMOSFET with strained channel	μ_{eff}, E_{eff}, I_D, V_D, V_{GS}, L, W and Q_{inv}.	Surface channel devices show low-field mobility enhancements of 80% at room temperature and 12% at 10 K, when compared to bulk Si.	Buried channel devices show peak room temperature mobilities about three times that of control devices.

VI. CONCLUSION

The review of strained Si channel metal oxide field effect transistors and their relative enhanced performance have been analysed. Є-Si MOSFETs are more popular in designing of VLSI circuit to achieve better performance. In this paper we reviewed the effect of strain in device structure and how it relates to the mobility and drain current improvement. It is expected that review of this study will help for further research and fabrication of fastest devices to use strained Si MOSFETs in electronics.

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