READ STABILITY ANALYSIS OF LOW VOLTAGE SCHMITT TRIGGER BASED SRAM

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Abstract - Ultra-low voltage operation of memory cells is relevant due to its applications in very low energy computing and communications. Due to parameter variations in nanoscaled technologies, stable operation is critical for the success of low voltage SRAMs. The proposed Schmitt Trigger (ST) based SRAM bit cells address the incompatible design requirement of conventional 6T SRAM cell. ST based SRAM cell incorporate built-in feedback mechanism in order to attain process variation tolerance which is necessary for future nano-scaled technology nodes. It also provides better read-stability compared to the standard 6T SRAM bit cell. The proposed circuit was implemented in Mentor Graphics Design Architect, simulated using Mentor Graphics ELDO at various supply voltages using TSMC 180nm technology.

Keywords: Low voltage SRAM, Schmitt Trigger, Read stability, Read SNM

I. INTRODUCTION

Memories are systems that store large amounts of information and are integral part of most of the digital devices. Reducing power consumption of memory is relevant as to improve the system performance, efficiency and reliability. SRAM is widely used in most of the embedded and portable devices because of their speed, ease of use and low stand by leakage.

Static Random Access Memory (SRAM) is a type of semiconductor memory that uses internal feedback to retain its data as long as power is applied. The one bit memory cell in SRAM consists of simple latch circuit with two stable states. A low power SRAM cell may be designed using cross coupled CMOS inverters as storage element.

Conventional 6T SRAM cell have difficulty in meeting growing demand of large memory capacity in various applications. Also Conventional 6T SRAM cell gives poor stability at reduced feature size and low supply voltages. With each technology generation, scaling of CMOS devices results in random variations in device parameters like threshold voltage etc. Low power SRAM cell results in significant degradation in SRAM cell data stability. This limits the SRAM operation in low-voltage regime employing minimum-sized transistors [1],[2].

In a given process technology, the minimum SRAM supply voltage is limited by increased sensitivity of circuit parameters and increased process variations while the maximum supply voltage is determined by process constraints such as gate oxide thickness[3]. To enable the SRAM bit cell to operate in wide voltage range minimum supply voltage has to be reduced further. With supply voltage scaling and increased process variations it leads to memory failures such as read, hold failure and write failure.
Conventional 6T SRAM cell gives poor stability during read operation so it is relevant to consider these issues during memory cell designs.

In this paper, ST based SRAM cell with built-in feedback mechanism is used in order to attain process variation tolerance which is necessary for future nano-scaled technology nodes.

The remainder of this paper is organised as follows. Section 2 describes various types of existing SRAM cells. Section 3 presents a brief review of conventional 6T SRAM cell. Section 4 briefly presents CMOS Schmitt trigger. Section 5 introduces the design of proposed Schmitt trigger and Schmitt trigger based SRAM cell. Section 6 presents the measurement results. Finally, conclusion is drawn in section 7.

II. RELATED WORKS

Several SRAM cells have been proposed with different aims like bitcell area, density, architectural timing specifications and low voltage operation. In four transistor (4T) bitcell, PMOS are used as access transistors[4]. For maintaining data ‘1’ reliably, the basic design requirement is such that PMOS OFF state current must be greater than pull-down NMOS transistor leakage current. Satisfying this design requirement over different voltage, process and temperature conditions may be challenging due to increasing process variations and exponential dependence of the sub-threshold current on threshold voltage. 5T SRAM cell uses single bitline and consist of asymmetric cross coupled inverters[5]. Here for read and write operations separate precharge voltages are required. It requires dc-dc converters and tracking read precharge voltage across different voltage, process and temperature conditions requires additional design margins in cell sizing. This may limits its applicability. The 6T SRAM cell contains a pair of weak cross-coupled inverters holding the state and a pair of access transistors to read or write the state. A single-ended 6T cell uses transmission gate instead of access transistor at one side [6]. By modulating the virtual VCC and virtual VSS of one of the inverters, write-ability can be achieved. Single ended 7T bitcell consists of single ended write operation and a separate read port[7]. The write operation in this single ended 7T bitcell needs either differential VSS or VCC or asymmetrical inverter characteristics. To overcome the problem of data storage destruction during the read operation, 8T-cell implementation was proposed for which separate read/write bit and word signal lines are used to separate the data retention element and the data output element[8]. In turn, the cell implementation provides a read-disturb-free operation. However, this implementation uses eight transistors, which results in a cell area increase of 30% in comparison to the conventional 6T-cell design. In single ended 9T bitcell, separate read port is used to decouple read and write operation[9]. Here to reduce the bit line voltage, stacked read access transistors are used. Single ended 10T bitcell, except for read port configurations it is similar single-ended 8T bitcell. To control read bitline leakage additional transistors can be used. In single ended transmission gate 10T bitcell, contents are buffered using inverter and whenever bitcell is accessed, it is transferred to read bitline[10].

In all of the previously reported bitcells, cross coupled inverter pair is the basic element for data storage. Here extra transistors were added to decouple read and write operation. For improving the stability of inverter pair operating at ultralow supply voltage none of the above reported bit cells incorporate process variation tolerance. Thus stability of the inverter pair is important for successful operation under PVT variations. Device sizing can be adopted to mitigate the effects of process variations however, at very low supply voltages it is not an effective method for improving the cell stability.

Hence, a different approach is needed in nano-scaled technologies for successful low voltage SRAM operation. In this work, Schmitt trigger based SRAM bit cell with positive feedback is introduced that exhibits process variation tolerance. This robust operation can be essential for SRAM scaling into future nanoscaled technologies.
III. CONVENTIONAL 6T SRAM CELL

In SRAM cell, the basic element used for data storage is the cross coupled inverter. Here, the output of one inverter is connected as input to other and vice-versa. The outputs of these inverters are connected to two access transistors which are connected to the bitlines. During read operation, the bitlines are pre-charged high and the word line is raised. When word line is raised, either BL or BR pulls down indicating the data value stored. The read operation results in formation of voltage divider network consisting of access and pull down transistors and this result in increase of voltage in the node storing logic 0. This corrupts the logic value stored in the cell and is defined as read failure [11].

![Fig.1. Conventional 6T SRAM cell [12](image)](image)

Also at low supply voltages the conventional 6T SRAM cell gives poor stability during read operation.

IV. CMOS SCHMITT TRIGGER

In order to satisfy the conflicting design requirements in conventional SRAM cell, Schmitt Trigger (ST) principle can be applied for the cross coupled inverter pair [12]. Schmitt Trigger is basically a comparator circuit with positive feedback [11]. When input is higher than a threshold value output is high, when input is less than lower threshold output is low and between these input values output retains its state. Thus, the noise immunity of conventional Schmitt Trigger is higher than that of an inverter. Therefore, Schmitt Trigger is basically an inverter circuit with two extra transistors that provide hysteresis.

![Fig.2. Conventional CMOS Schmitt Trigger [13](image)](image)

In the double transistor inverter, the transistors P2 and N2 have high threshold voltage than P1 and N1 due to body bias effect. The addition of two transistors P3 and N3 provides hysteresis such that the output switches to high to low or low to high only after the ON condition of N2 or P2 respectively [11]. When input voltage is zero, N1 and N2 in OFF condition while P1 and P2 are in ON condition and output is at logic HIGH. When input voltage reaches the threshold voltage of N1, then N1 will be ON, while N2 OFF and output at logic high makes N3 ON. N1 tries to pull down the node between N1 and
N2 while N3 tries to pull up the node to a voltage $V_{DD}-V_T$ so N2 keeps the output at logic HIGH. When input switches to threshold voltage of N2 output switches to logic LOW and thereby switching point voltage is increased [11]. Thus, depending upon the direction of input transition, Schmitt Trigger increases or decreases the switching threshold of the inverter using feedback mechanism [13].

V. PROPOSED SCHMITT TRIGGER BASED SRAM

This above structure can be used to form the inverter of our SRAM cell. But this requires six transistors instead of two transistors thereby 14 transistors in total to form the SRAM cell and that result in large area. The feedback mechanism in PMOS pull-up is not used because PMOS transistors are used as weak pull-ups to hold 1 state. Hence feedback can be used only in pull down logic. The modified ST schematic is as shown in fig.3. During 0 to 1 input transition, the feedback transistor tries to keep the output at logic HIGH by increasing the source voltage of pull down transistor N2. This leads to higher switching threshold of the inverter with sharp transfer characteristics.

![Proposed Schmitt Trigger](image1)

This gives robust read operation since read failure is initiated by the 0 to 1 input transition. Feedback mechanism is not present during 1 to 0 input transition and results in smooth transfer characteristics that is essential for write operation. Thus, Schmitt Trigger improves both write stability and read stability of SRAM cell.

In the proposed Schmitt Trigger based SRAM cell, feedback mechanism is used in pull down network as shown in fig.4. Transistors PL-NL1-NL2-NFL forms the one inverter while transistors PR-NR1-NR2-NFR forms the other Schmitt Trigger inverter.

![Schmitt Trigger based SRAM cell](image2)

Depending upon the direction of input transition switching threshold of the inverter is changed by positive feedback from feedback transistors (NFL/NFR). During read operation, with $V_L=0$ and $V_R = V_{DD}$, the voltage of VL node rises due to voltage divider action between pull down NMOS transistor and access transistor. This leads to read failure if this voltage is higher than switching threshold of the
other inverter. So, in order to avoid read failure, the feedback mechanism increases the switching threshold of the inverter PR-NR1-NR2. Thus the voltage at the node VNR is raised by transistors NR2 and NFR storing logic high at the output.

Thus the logic state of the memory cell is preserved by Schmitt Trigger action. The proposed Schmitt Trigger based SRAM cell utilizing differential operation gives better read stability.

VI. RESULTS AND DISCUSSION

In order to understand the effectiveness of the proposed design, the performance of the proposed design is evaluated against conventional design. The compared designs include conventional 6T SRAM and Schmitt Trigger (ST) based SRAM. The Pyxis schematic of Mentor Graphics is used in order to create the schematics of the circuit. The performances of both conventional and proposed designs are evaluated through pre-layout simulations using Eldo simulator. The output waveforms are viewed using E-Z wave viewer. The target technology is the TSMC 180-nm CMOS process.

6.1 READ SNM

The stability of the cell is quantified by Static Noise Margin (SNM). SNM measures maximum dc voltage that the cell can tolerate before it changes its state. Graphical method can be used to determine the SNM of SRAM cell. The voltage transfer curve (VTC) of one inverter is super imposed with VTC of other inverter to obtain butterfly curve. SNM is determined from the length of side of square that can be inscribed between the two curves.

![Fig.5. Simulation setup of conventional 6T SRAM Cell](image)

Fig.5 shows the schematic diagram along with simulation setup of 6T SRAM in Pyxis schematic editor window.

The proposed ST based SRAM cell incorporate built-in feedback mechanism in order to attain process variation tolerance provides better read-stability compared to the standard 6T bit cell. Fig.6 shows the schematic diagram along with simulation setup of Schmitt Trigger based SRAM in Pyxis schematic editor window.

![Fig.6. Simulation setup of Schmitt Trigger based SRAM Cell](image)
To find RSNM, the cell ratio (CR) must be properly selected. Here, the word line and bit line is kept high and then the feedback between these two inverters is broken. The voltage transfer characteristic (VTC) of the half cell is plotted between output and input voltage by DC analysis. Thus, butterfly curve is obtained by super imposing VTC of one inverter with VTC of other inverter of the SRAM cell. SNM is determined from the length of the side of the largest square that can be inscribed between the curves.
Fig. 9. (a) RSNM of ST SRAM Cell for 2.5 V

Fig. 9. (b) RSNM of ST SRAM Cell for 1.8 V

Fig. 9. (c) RSNM of ST SRAM Cell for 1.4 V

Fig. 9. (d) RSNM of ST SRAM Cell for 1 V
The table compares Read SNM of Conventional 6T SRAM and Schmitt Trigger based SRAM cell. From the result it is clear that as supply voltage decreases 6T SRAM fails in read operation below 100mV. Also, at same cell ratio the RSNM of ST based SRAM is more than conventional 6T SRAM cell at dynamic voltages.

**Table 1: Supply Voltages VS RSNMs**

<table>
<thead>
<tr>
<th>$V_{DD}(V)$</th>
<th>RSNM (mV) (6T SRAM Cell)</th>
<th>RSNM (mV) (ST SRAM Cell)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.5</td>
<td>380</td>
<td>570</td>
</tr>
<tr>
<td>1.8</td>
<td>240</td>
<td>370</td>
</tr>
<tr>
<td>1.4</td>
<td>220</td>
<td>350</td>
</tr>
<tr>
<td>1</td>
<td>200</td>
<td>250</td>
</tr>
<tr>
<td>0.6</td>
<td>110</td>
<td>160</td>
</tr>
</tbody>
</table>
Graphical comparison of conventional and ST SRAM is as shown in fig.10.

<table>
<thead>
<tr>
<th>VDD (V)</th>
<th>RSNM (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.4</td>
<td>70</td>
</tr>
<tr>
<td>0.2</td>
<td>20</td>
</tr>
<tr>
<td>0.1</td>
<td>0 (READ FAILURE)</td>
</tr>
</tbody>
</table>

Fig.10. Comparison between Read SNM of Conventional 6T SRAM and ST SRAM cell

Simulation results show that 6T SRAM fails below 100mV in read operation. Thus, from above results it is clear that the proposed design outperforms conventional design.

VII. CONCLUSION

In this work, evaluation of Schmitt Trigger based SRAM for ultra low voltage operation is performed. The built in feedback mechanism in the proposed Schmitt Trigger based design is found to be effective for process tolerant, low voltage operation in future nanoscaled technologies. It can be concluded from the simulation results that as supply voltage decreases, RSNM of conventional 6T SRAM is found to be 0 at VDD= 0.1v due to process variations while ST based SRAM is still stable at this voltage. Also, at same cell ratio the RSNM of ST based SRAM is more than conventional 6T SRAM cell at dynamic voltages. This implies ST based SRAM cell can work efficiently in sub-threshold region.

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REFERENCES


