STUDY OF VOLTAGE AND CURRENT SENSE AMPLIFIER

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Abstract—Performance of sense amplifier has considerable impact on the speed of caches used in microprocessors. The small difference in voltage level of bit lines of memory cell is amplified by sense amplifier. Voltage mode sense amplifier reduces the power dissipation during read and increases the speed also. This paper describes voltage mode sense amplifier and current mode sense amplifier and compare their power dissipation and time delay. Current sense amplifier is independent of bit line capacitance and it ia better choice in high density RAM. Delay of voltage mode increases with bit line capacitance.so it is a better choice.

Keywords: SRAM, Delay ,Power Dissipation, Bit lines, VSA,CSA.

I. INTRODUCTION

Technology and supply voltage scaling continues to improve the logic circuit delay with each technology generation. However, the speed of the overall circuit is increasingly limited by the signal delay over long interconnects and heavily loaded bit-lines due to increased capacitance and resistance [1]. SRAM design is constrained by its compact area requirement, which forces the use of near minimum sized transistor for the memory cell design. The small memory cell must drive large capacitive bit-lines resulting in a very small signal swing. This will limit the speed of any sensing scheme that requires a development of specific level of differential voltage to initiate the sensing operation. The key strategy to overcome the speed limitation may have to focus on diminishing the bit-line swing to reduce both the delay and energy involved in charging and discharging the bit-lines [2]. The small signal swing of bitlines involves a circuit design of sense-amplifiers, which can sense the signal reliably at a high speed.

From the past few decades, the growth of the electronics industry is very fast and also the use of integrated circuits in computing, telecommunications and consumer electronics. In the 1958, there was only a single transistor on the chip called single transistor era and at present day ULSI (Ultra Large Scale Integration) systems with more than 50 million transistors in a single chip. Today the size of the memory is decreasing and the storing capacity is increasing. As the storing capability increased, the time response for the data writing and reading from the memory should be very fast. The speed gap between the MPUs and memory devices has been increased in the past decade. The MPU speed has improved by a factor of 4 to 20 in the past decade. On the other hand, in spite of the exponential progress in storage capacity, minimum access time for each quadrupled storage capacity has improved only by a factor of two. In the memory, it is common to reduce the voltage swing

II LITERATURE SURVEY OF VARIOUS SENSE AMPLIFIERS

On the basis of their working, Sense amplifier may be classified as follow:
1. Voltage Sense Amplifier
2. Current Sense Amplifier
3. Charge Transfer Sense Amplifier (CTSA)
The simplest voltage sense amplifier is the differential couple. When a cell is being read, a small voltage swing appears on the bit line which is further amplified by differential couple and used to drive digital logic. However, the bit line voltage swing is becoming smaller and is reaching the same magnitude as bit line noise, the voltage sense amplifier becomes unusable.

The fundamental reason for applying current mode sense amplifier in sense circuit is their small input impedances. Benefits of small input and output impedances are reductions in sense circuit delays, voltage swings, crosstalk, substrate currents and substrate voltage modulations.

The operation of the CTSA is based on the charge redistribution mechanism between very high bit line capacitance and low output capacitance of the sense amplifier. A differential charge transfer amplifier takes advantage of the increased bit-line capacitance and also offers a low-power operation without sacrificing the speed.

III VOLTAGE SENSE AMPLIFIER

Sense amplifier which detects the voltage difference on the bit lines is called voltage mode sense amplifier. There are some voltage mode sense amplifiers like single ended sense amplifiers, differential amplifiers and current mirror sense amplifiers. Different types of sense amplifier are used in different types of memory cells according to the proper design and efficient performance. According to the characteristics of the amplifiers, they are used in the design.

Sense amplifier is the main part of the memory design. Voltage mode sense amplifiers detect the low voltage level signal from the bit lines and produce a high swing signal as an output. A design circuit of voltage mode sense amplifier is shown in Figure 4.9. In this, transistors M5 and M6 are the input transistors. The circuit is connected to the ground through transistor M9. The gate of this transistor is connected with the transistors M7 and M8. A clock is applied on the input of these transistors.
The output of the voltage mode sense amplifier is shown in the given below graph. V(S0) and V(S0N) are the two outputs which are shown by green and yellow colour. This output of voltage mode sense amplifier is without bit line capacitance.

**IV CURRENT SENSE AMPLIFIER**

Current mode sense amplifier is used to detect the current difference between the bit lines to determine whether a ‘1’ or ‘0’ is stored in the memory cell. It directly measures the cell read current and transfers it to the output circuits. This approach can overcome the restriction of gain reduction brought on by
voltage mode sense amplifier at low power supply voltage. The simplest structure of the current mode sense amplifier is described in the following. The conventional current sense amplifier basically consists of four equal sized PMOS transistors as shown in Figure 2.9. It features a current sensing character since it represents a virtual short circuit to the bit lines, which transfer the cell current directly to the output circuits [4].

Suppose the cell is accessed and, storing a logic “0” in the cell, it draws a current I. The gate source voltage of MP1 will equal that of MP3 since their currents are equal, their sizes are equal, and both transistors are in saturation. This voltage is represented by V1. The same applies to MP2 and MP4. Their gate voltages are represented by V2. It follows that if grounded, the left bit line will have voltage V1+V2, and the right bit line will also have voltage V1+V2. Therefore the potentials of the two bit lines will be equal and independent current distribution. This means that there exists a virtual short circuit across the bit lines. Since the bit line voltages are equal, the bit line load currents will also be equal. As the cell draws current I, the right hand leg of the sense amplifier must pass more current than the left leg. The drain currents of MP3 and MP4 are passed through the current conveyor is therefore equal to the cell current. But if a logic ‘1’ is stored in the cell, a current would then flow out of the cell and cause the left hand leg to pass more current than the right hand leg. This difference in current implies a logic ‘1’ is being stored in the cell.

Owing to an intrinsic precharge property, current consumption for the current sense amplifier decreases, yet sensing speed improves. The virtual short circuit character ensures equal bit line voltages, thus eliminating the need for bit line equalization during a read access. The sensing delay is insensitive to bit line capacitances since no capacitor discharging is required to sense the cell data. Therefore, current sense amplifier has better performance than voltage sense amplifier in terms of smaller delay and less current consumption [4].
The delay of the voltage mode sense amplifier increases as increases of the capacitances. So, voltage mode sense amplifier is not the perfect choice where the time is primary concern. This designed sense amplifier is based on the current mode approach. The sensing speed is independent of the bit line and data line capacitances and a separated positive feedback technique is employed to give the circuit high speed, low power operation. As the density of memory devices increases, certainly the associated parasitic capacitances also increase. Large capacitive loads cause a major sensing delay in memory devices, so high speed sense amplification of small memory cell signals is the key to achieving a fast access time in SRAM. Conventional sense amplifiers are based on voltage sensing techniques, which are sensitive to parasitic capacitance. Recent approaches to designing sense amplifiers employs current sensing techniques the advantages in term of speed are obvious and very attractive.

V. POWER REDUCTION TECHNIQUES

Any circuit used in the designing is preferred on the basis of its characteristics, so the circuit should have high speed, gain, less delay, and less power dissipation. There are different techniques which are used for the low power dissipation

**MULTITHRESHOLD-VOLTAGE CMOS (MTCMOS)**

Would The multithreshold-voltage CMOS (MTCMOS) circuit was proposed by inserting high threshold devices in series into low $V_{th}$ circuitry. Figure 3.2 shows the schematic of an MTCMOS circuit. A sleep control scheme is introduced for efficient power management.

Two high VT transistors are used, high VT PMOS is connected to the power supply, where NMOS is connected to the ground. Due to these transistors a virtual power supply and ground are appeared respectively on the drain terminal nodes of the both transistors. In the active mode, SL is set low and sleep control high $V_{th}$ (MP and MN) are turned on. Since their on resistance are small, the virtual supply voltage ($V_{DDV}$ and $V_{SSV}$) almost function as real power lines. In the standby mode, SL is set high, MN and MP are turned off and the leakage current is very low. In this only one type of high $V_{th}$ transistor is enough for leakage control [5].
**VARIABLE THRESHOLD CMOS (VTCMOS)**

Variable threshold CMOS (VTCMOS) is a body biasing design technique. Figure shows the VTMOS scheme. In order to achieve different threshold voltages, a self substrate bias circuit is used to control the body bias. In the active mode, a nearly zero body bias is applied. While in standby mode, a deeper reverse body bias is applied to increase threshold voltage and to cut off leakage current. Furthermore, in active mode, a slightly forward substrate bias can be used to increase the circuit speed while reducing short channel effect.

**DYNAMIC THRESHOLD CMOS (DTCMOS)**

For dynamic threshold CMOS, the threshold voltage is altered dynamically to suit the operating state of the circuit. A high threshold voltage in the standby mode gives low leakage current, while a low threshold voltage allows for higher current drives in the active mode of operation.

Dynamic threshold CMOS can be achieved by tying the gate and body together DTMOS. Figure shows the schematic of a DTMOS inverter. DTMOS can be developed in bulk technologies by using triple wells. Stronger advantage of DTMOS can be seen in partially...
depleted Silicon-on-Insulator (SOI) devices. The supply voltage of DTMOS is limited by the diode built-in-potential. The $pn$ diode between source and body should be reverse biased. Basically, this technique is only suitable for ultra-low voltage (0.6 and below) circuits [5].

IV CONCLUSION
The voltage mode sense amplifier circuit has been designed and simulation has been done on Tanner tool. A delay of 9.5ns and power dissipation of 232μW was found. Next, the current mode sense amplifier has been designed. From the simulation results it is found that the net delay of sense amplifier is 8.2ns and power dissipation is 0.9μW. This shows a significant improvement in delay and power dissipation in comparison of the voltage mode sense amplifier.

REFERENCES
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