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Alleviation of Voltage dip in High Voltage Transmission Line using DVR with EZSI

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Abstract— Compensation of load side voltage design and implementation of a topology of Dynamic Voltage Restorer with Embedded Z- source Inverter which is capable of compensating voltage sag and voltage swell at sensitive load terminals. Depend on this; the DVR consists of uncontrolled rectifier for giving DC supply to Embedded Z source inverter through DC link. This topology is proposed in order to improve the voltage restoration property in high voltage transmission line. By controlling the over shoot through EZI provide ride-through capability during voltage sag, swell and high reliability. With the help of hysteresis controller the restored voltage will be injected in line. The simulation results are presented to manifest the effectiveness of the proposed DVR system, which exhibits the compensation for voltage sag and swell mitigation.
Index Terms- Dynamic Voltage restorer (DVR), Hysteresis Voltage controller, Embedded Z- Source Inverter (EZI).

I. INTRODUCTION

The requirement of the electrical power is increasing and at the same time transmitting the power through the distribution system are also have more problems. Voltage variations are one of the most severe problems in power quality to be managed. There are several types of voltage fluctuations that can creates the system to malfunction, like surges, spikes, sag, swell, harmonic distortions, and momentary disruptions. Power quality, is very difficult to quantify like quality in other. Among them, voltage sag and swell are the major power quality problems in the transmission line. Voltage swell is the sudden increase of voltage in supply voltage, whereas the voltage sag is the sudden decrease in supply voltage. This is caused due to the sudden reduction or addition of the load across that particular feeder. This sudden disturbance of voltage is atoned by injecting the voltage in series with the supply from another feeder at the time of disturbances using DVR. Solid state devices hold substantial promise for making distributed energy applications more efficient and cost effective. The application of dynamic voltage restorers (DVR) on power distribution systems for suppression of voltage sags/swells at demanding loads. DVR is one of the compensating types of custom power devices. The ZS converters are distinct from conventional converters like the VSI and CSI. Because of a unique X-shaped impedance network on its DC side, interfaces the source and the inverter Hbridge. It facilitates both buck and boosting the voltage. Therefore, Z- source converters are less consequence in an apparent, and can be designed with inductor and capacitor elements no special device required. Believing in the prospects of Z-source inverters, introducing a new family of embedded EZ-source inverters can produce the same gain as the Z-source inverters, but with smoother and smaller current / voltage maintained across the DC input source and within the impedance network. These latter features are attained without using any additional passive filter, which surely is a favorable advantage since an added filter will raise the system cost, and at times can complicate the dynamic tuning and resonant consideration of the inverters. This system configuration allows the use of an extremely small dc capacitor intended for smoothing the common dc-link voltage. During voltage sag, the DVR injects a voltage to restore the load supply voltages. In this way, DVR deals active and reactive power with the external system. If active power is supplied to the load from the DVR, it needs a source for this energy. Four types of system are available; here DVR with no storage and load-side-connected shunt converter is considered. The Hysteresis loop control method adopted for DVR

injection voltage control can have similar characteristic as the Proportional integral controller, with high gains at both the positive and negative line frequencies (±50 Hz), and would thus give almost zero steady-state error for the positive- and negative sequence components control for unbalanced voltage regulation by proper selection of the weighting functions along with explicitly specified degree of robustness in the face of parameter variations. An inner current feedback loop is also employed for transient and stability improvement. The multi-loop DVR controller would guarantee both good transient performance and steady-state error tracking. The design of the DVR voltage control is consists of two loops; they are Hysteresis outer voltage loop and Hysteresis inner current loop. Similar to a typical multi-loop control design approach, the DVR controller design is an iterative process. A Hysteresis loop controller is first designed with specified robustness and error tracking performance based on a given plant including inner current loop. The inner current regulator is then fine-tuned with consideration of its influence on the synthesized Hysteresis loop controller and the generated new plant (for the outer loop), and its relations to load current disturbance rejection capability. After the inner current loop regulator gain is determined, a Hysteresis voltage controller is finally obtained (redesigned) based on the best-tuned inner current loop. Based on the reference voltage and distorted voltage, the error voltage generated as pulse signals. This pulse signals given to switches of the Z source inverter, it gets injected compensated voltage.

II. BASIC OPERATION OF DVR

Dynamic voltage restorer (DVR) is a series connected flexible ac transmission systems (FACTS) devices used to compensate voltage sags and swells during aberrant conditions in the distribution systems. DVR is one of the most effective FACTS for “restoring” the quality of voltage at its load-side terminals when the voltage at its source-side terminals is disturbed. As problems such as the voltage sag, swell happens; DVR protects the sensitive loads by restoring the load side voltage dynamically. Here load side compensation is employed. The load voltage is taken to uncontrolled rectifier in order to convert the ac voltage into dc voltage. This dc voltage is given as supply to the ZSI through the DC link capacitors. Generally, the conventional DVRs consist of series voltage sources (VSI), series injection transformer and energy source unit. The VSIs are greatly used in DVRs due to their proper output voltage with low harmonics level. The main disadvantage of these inverters is their buck type voltage characteristics limiting the maximum output voltage that can be attained. The Z-source inverter has been an alternative to existing inverter topologies with many inherent advantages. It facilitates both voltage-buck and boost capabilities. They are immune to EMI noise thus greatly increases the reliability.

Injected voltage (V_C) is in quadrature with the load current. To raise the voltage at the load bus, the voltage injected by the DVR is capacitive and V_L leads V_{S1}. In figure it shows the in-phase compensation for comparison. The current phasor is determined by the load bus voltage phasor and the power factor of the load to recognize.

Implementation of the minimum energy compensation requires the measurement of the load current phasor in addition to the supply voltage. When, V_C is in quadrature with the load current, DVR supplies only reactive power. However, full load voltage compensation is impossible only when the supply voltage is above a minimum value that depends on the load power factor.

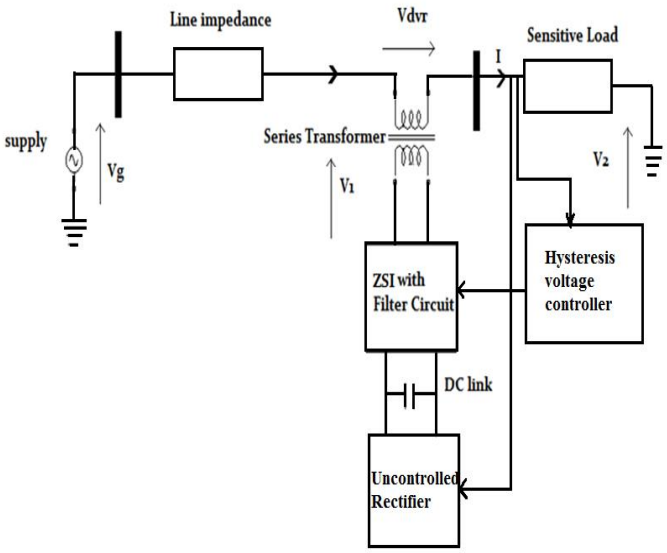

Fig. 1: Schematic diagram of a DVR System

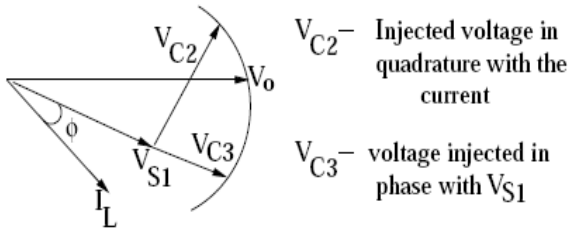

Fig. 2: In-Phase Compensation phasor Diagram

$$V_s^{\min} = V_0 \cos \qquad \textbf{(1)}$$

When the magnitude of V_C is not constrained, the minimum value of V_S that still allows full compensation is Where Á is the power factor angle and V_o is the required magnitude of the load bus voltage. If the magnitude of the injected voltage is limited, the minimum supply voltage that allows full compensation is given by

$$V_s^{\min} = V_0 \cos . V_s^{\min} = \left[V_0^2 . V_c^{\max} . \sin + \left(V_c^{\max} \right)^2 \right] \textbf{(2)}$$

Note that at the minimum source voltage, the current is in phase with V_S for the case (a).

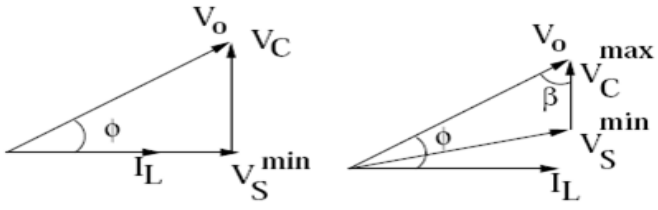

Fig. 3: Phasor diagrams determining $V_s^{\min}$ with quadrature injection

If the source voltage magnitude is less than $V_s^{\min}$, the DVR has to supply non-zero energy to provide full compensation. But it is possible to devise a strategy that results in minimum energy requirement for full compensation. The system impedance (Z_{TH}) depends on the fault level of the load bus. When the system line voltage (V_{TH}) drops, the DVR starts immediately and injects a series voltage V_{DVR}

through the injection transformer so that the rated magnitude of load voltage V_L can be maintained. The series injected voltage of the DVR can be written as

$$V_{DVR} = V_L - Z_{TH}.I_L - V_{TH} \quad \textbf{(3)}$$

Where

V_L : The desired load voltage magnitude

Z_{TH} : The load impedance.

I_L : The load current

V_{TH} : The system voltage during fault condition

The load current IL is given by,

$$I_L = \frac{[P_L + jQ_L]}{V} \quad \textbf{(4)}$$

The complex power injection of the DVR can be written as,

$$S_{DVR} = V_{DVR} * I_L^* \quad \textbf{(5)}$$

III. PROPOSED SYSTEM

The DVR consists of mainly an EZI; no filter is required to regulate the output voltage of ZSC. The DVR injects ac voltage in synchronism with the supply voltage. The supply voltages have controllable amplitude, phase angle and frequency which enable the DVR to restore the quality of the voltage at the load side when the supply voltage is distorted. A shunt converter is connected to the load side is uncontrolled charged rectifier. The load may be linear or non-linear. The output of rectifier supplied to DC-DC Step up converter (dc voltage). This output voltage get boosted can feed the E Z-source inverter, which is connected in series to the power supply through series transformer. The impedance network is used to boost or buck the input voltage depends on the boosting factor. Three phase supply voltage is taken to the hysteresis controller. Where, they get compared with the reference voltage for the detection of voltage distortion. Based on the error signal it generates digital pulses. Hysteresis controller produced controlled switching pulses to EZI. Where, the hysteresis controller can control the voltage sag, swell & harmonic by producing PWM signal based on the error with their reference voltage. The injection transformer provides the isolation between load and system.

3.1. DETECTION OF SAGS / SWELL IN THE SUPPLY VOLTAGE

In this study, monitoring of V_d and V_q is used to return the magnitude and phase voltage of load to the magnitude and phase reference load voltage. The three-phase supply voltage is connected to a conversion block that convert to rotating frame (d q) with using a software based Phase – Lock Loop (PLL). Three-phase voltage is transformed by using Park transform, from a-b-c to o-d-q frame

$$\begin{bmatrix} V_d \\ V_q \\ V_0 \end{bmatrix} = P \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix}$$

$$P = \begin{bmatrix} \cos\theta & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta - \frac{4\pi}{3}\right) \\ \sin\theta & \sin\left(\theta - \frac{2\pi}{3}\right) & \sin\left(\theta - \frac{4\pi}{3}\right) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix}$$

$$\theta = \theta_0 - \int_0^t wt.dt$$

The detection block detects the occurrence of voltage sag or swell. If occurs, this block generates the reference load voltage. The sag detection scheme is based on root means square (rms) of the error vector. Closed loop load voltage feedback is added, and which is incorporated in the frame in order to minimize any steady state error in the fundamental component. The injection voltage is also developed according to the difference between the reference and the supply voltage and the error will be applied to the EZI to produce the preferred voltage, by using the Hysteresis Voltage Control.

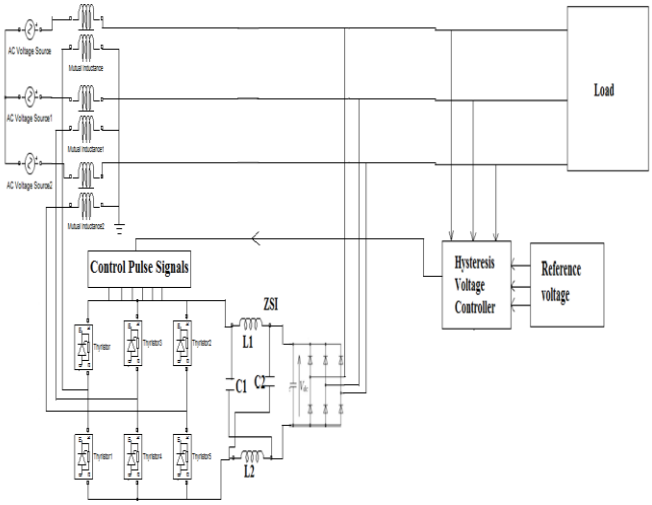

Fig. 4: Modeling of Proposed system

3.2. Hysteresis Voltage Control

In this paper, hysteresis voltage control is used to improve the load voltage and determine triggering signals for inverters gates. A basic of the hysteresis voltage control is based on an error signal between an injection voltage (V_{inj}) and a reference voltage of DVR (V_{ref}) which produces required control signals. The Hysteresis Band (HB) is employed. When there is difference between the reference and inverter voltage reaches to the upper / lower limit, the voltage is forced to decrease / increase.

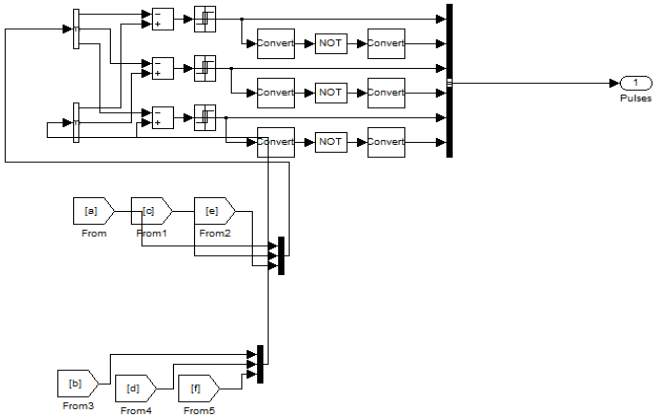

Fig. 5: Simulink Diagram of Hysteresis Controller

I.3. DC LINK

The energy storage unit consists of capacitor. The rectifier unit acts a source for EZI. The rectified output voltage is fed to the Impedance network of the EZI. The purpose is to supply the necessary energy to the EZI through a DC link for the generation of injected voltages. Ultra capacitors and Batteries are the common types of energy storage devices. In fact, the capacity of the stored energy directly determines the duration of the sag which can be mitigating by the DVR.

I.4. Z-SOURCE INVERTER (ZSI)

This ZSI employs a unique impedance network coupled with the inverter main circuit to the power source. The impedance network is used to buck or boost the input voltage depends upon the boosting factor. This network also acts as a second order filter. This should require less inductance, less capacitances and their sizes are in small. This impedance network, constant impedance output voltage supplied to the main circuit of three phase inverter. The inverter circuit consists of six switches. Gating signals are generated by the Hysteresis voltage controller.

There are three operating modes in Z-Source inverter.

Mode 1 - Six active vectors states.

Mode 2 - Two zero vector states.

Mode 3 – One shoot through vector state.

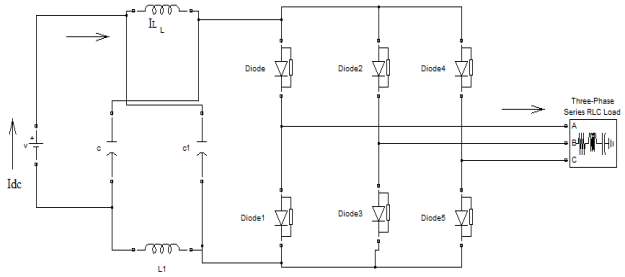

Fig. 6 Connection diagram for Active mode state of ZSC

When the dc voltage is impressed across the load the corresponding mode is called active mode state. Because, the direct supply voltage is given to the load through Z shape impedance network.

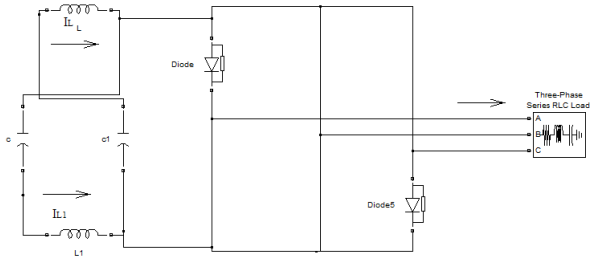

Fig. 7: Connection diagram for Zero mode state of ZSC

When, the load terminals are shorted through either the lower or upper three devices.

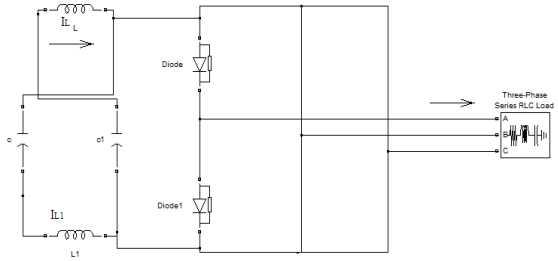

Fig 8 Connection diagram for Shoot through mode of ZSC

When, the inverter bridge is in one of the eight non shoot-through switching states (or vector) when the load terminals are shorted through both the upper and lower devices of any one phase leg (i.e., both devices are gated on), any two phase legs, or all three phase legs. This shoot-through zero state (or vector) is refused in the traditional V-source inverter, because it creates shoot-through. This third zero state (vector) shoot-through can be generated by seven different ways: shoot-through via any one phase leg, combination of any two phase legs, and all three phase legs. The EZI setup provides

the shoot-through zero state possible. This shoot-through zero state provides the unique buck-boost feature to the inverter.

IV. SIMULATION RESULTS

A 3Φ, 415V, 50 Hz supply (generating station) side can feed the two or more loads through distribution line. During transmission fault can be created, sudden load attachment or sudden removal of load causes distortion in supply voltage. Here due to over energization of load, voltage swell created. And due to fault occurrence either may be single or three phase fault causes the voltage sag. Here from the time 0.1s to 0.2s faults occurred in open loop 3Φ system, hence voltage get distorted.

In 3 phase distribution line due to fault, sag voltage get distorted to 30% (125V) at 0.1s. After clearing fault, the voltages get normalized to 415V at 0.2s. Here due to three phase fault, the voltage gets distorted as sag.

In distribution line, due to fault occurrence voltage distortion takes place. This can be avoided by using load side compensation DVR, with EZI instead of VSC. During fault occurrence time 0.1s the DVR get activated and can inject voltage of about distorted voltage.

This range of distortion can be detected by take voltage for sag detection or swell detection. With the help of HVL controller, we can compensate the voltage distortion. The fault gets cleared at 0.2s, that time DVR get deactivated.

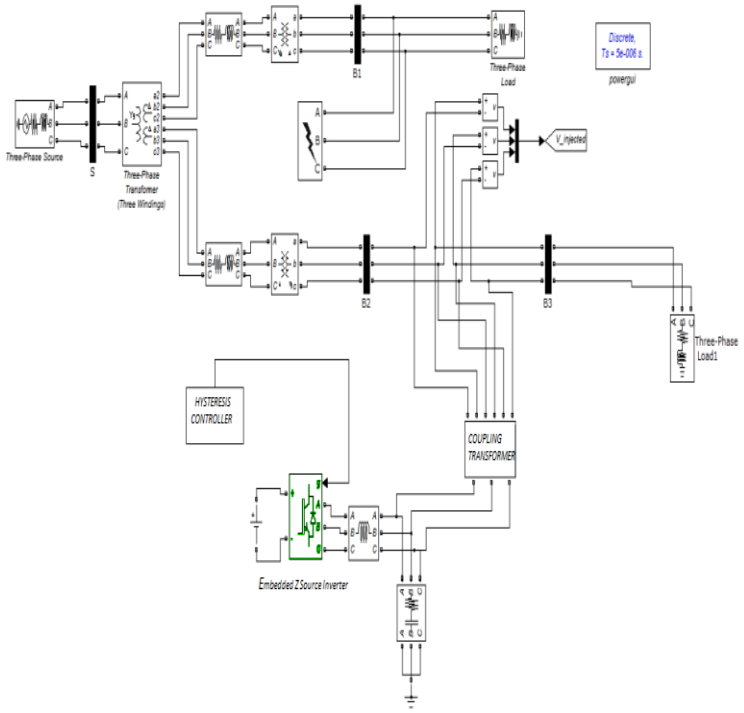

Fig. 9: Simulation of DVR System for Voltage Retention

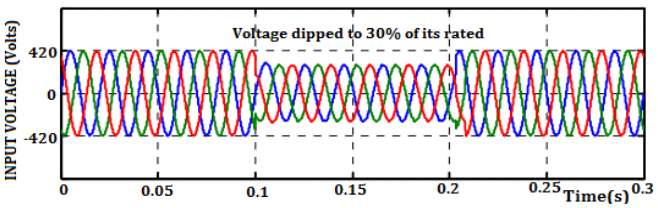

Fig. 10: Simulation of high line voltage with sag distortion

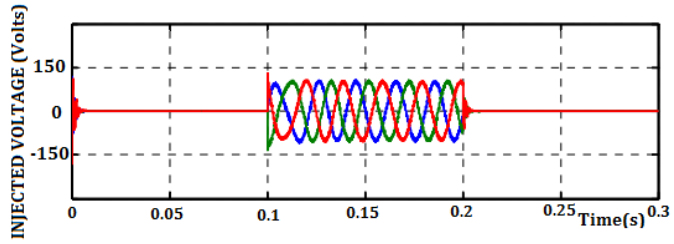

Fig. 11: Simulation of injecting voltage at line by DVR

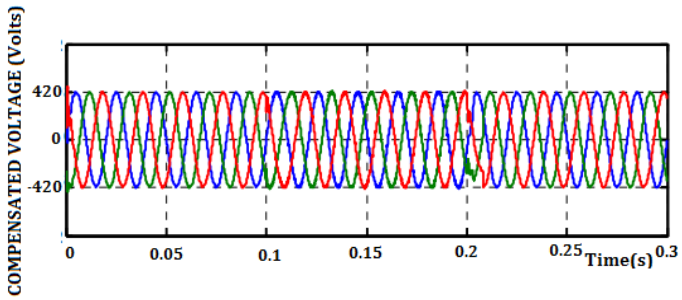

Fig. 12: Simulation of Load voltage: Compensated voltage after injected by DVR for sag distortion

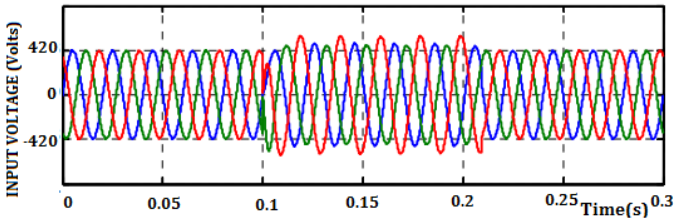

Fig. 13: Simulation of high line voltage with swell distortion

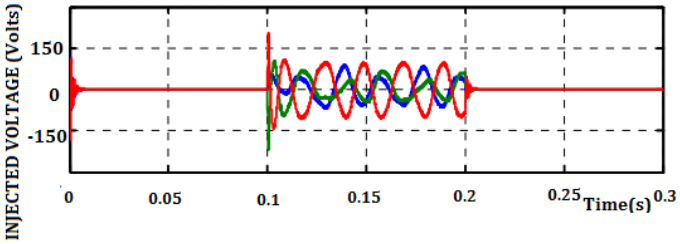

Fig. 14: Simulation of injecting voltage at line by DVR

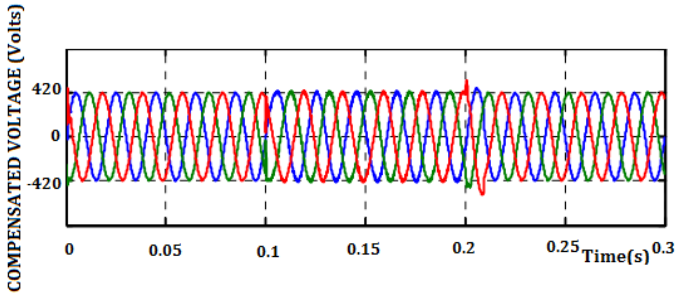

Fig. 15: Simulation of Load voltage: Compensated voltage after injected by DVR for swell distortion

IV. CONCLUSIONS

This project has proposed a DVR that compensate deep and long duration voltage sag, voltage swell by load side compensation of DVR. The DVR is based on a shunt rectifier fed series Embedded Z inverter through dc link. A method of incorporating voltage compensation capability to the DVR has been proposed using hysteresis voltage control.

A Hysteresis voltage controller was designed for DVR voltage regulation with explicit robustness in the face of system parameter variations. A proper selection of weighting functions would specify the robustness and error tracking performance, and the synthesized Hysteresis controller can be tuned with significant gains at positive and negative line frequencies so that it would effectively regulate the positive- and negative-sequence components. An inner current loop is also designed and embedded within the Hysteresis voltage loop. The design of the components of the DVR has been presented. Based on the design procedure, band controlled DVR is designed and further validated by simulation and experimental results.

In this project, 3 phase fault created at 0.1s and clear at 0.2s. During this fault time voltage distortion takes place, which recovered by DVR. This DVR get activated at 0.1s and inject the distorted voltage up to 0.2s. During sag distortion, the supply voltage 415V dipped to 125V at 0.1s. With the help of DVR compensator, the dipped voltage gets increase to supply voltage at 0.2s. Similarly, in swell distortion the supply voltage increased to 498V at 0.1s. With the help of DVR compensator, the voltage swells decrease to its supply voltage at 0.2s. Hence, with the help of load side compensating DVR we can achieve voltage regulation during fault time. Time domain simulations of the DVR is done, under different conditions including distorted supply voltage and distorted voltage sags, distorted voltage swell have validated the operation of the proposed DVR

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