



## A Survey of Different Topologies for Network-on-Chip Architecture

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**Abstract :** Network-on-chip (NoC) has emerged as an imperative aspect that determines the performance and power consumption of many-core systems. Different topologies have various advantages and applications. This paper presents a brief survey of various NoC topologies, and their related parameters.

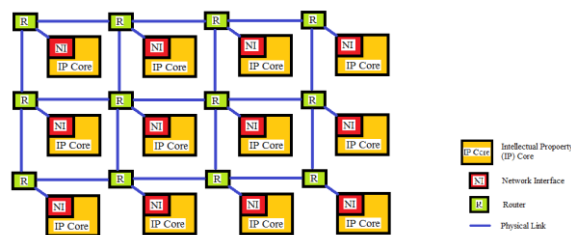
**Keywords—** Network-on-chip; NoC topologies; Topology Parameters.

### I. INTRODUCTION

In the recent years there has been a shift in the technology, the number of IP modules in a system-on-chip increase. This has led to poor performance of bus based systems; buses do not provide the required bandwidth, latency and power requirements for many application systems. When tens to hundreds of SoC systems are packed into one die, the hierarchical bus is not scalable and becomes the major throughput bottleneck. In such a scenario, Network-on-Chip (NoC) provide an efficient solution.

NoC has been proposed as a highly structured and scalable solution to address the communication problems in on-chip systems. NoC has several advantages over dedicated wiring and buses, e.g., high bandwidth, low-latency, low-power consumption and scalability[8]. NoCs can make SoCs more structured, and reusable, and can also improve their performance[3].

The generalized NoC architecture is as shown in figure1. In the figure the IP cores are connected in a mesh topology. The NoC consists of Intellectual Property (IP) Core, Network Interface (NI), Router and Physical Link. The way in which the IP core, NI, Router and Physical Link are connected we get different topologies. Some of the most commonly used topologies are described in the next section.



*Fig. 1 Generalized NoC Architecture*

The Intellectual Property (IP) Core is a reusable logic unit that can either be a processing element- such as CPUs or a storing element- such as RAM. The IP is the property of a third party designer and the implementation of IP is not a part of NoC design.

The Network Interfaces (NI) or Network Adapter (NA) is present between the IP core and the router. The main task of the NI is to convert the transaction requests into packets for injection into network. The

NI encapsulates the IP data with necessary header information which is required by the router for further processing.

The main task of the router is to route the data packets from source to destination. The routing decision is made with the help of decoding the information in the header and the implemented routing algorithm. The links form a critical part of NoC design. The two main types of connections usually required is between router-to-router and router-to-IP. There can be short length links between routers and IPs or global and semi-global links between routers and IPs.

## II. NoC TOPOLOGIES

Topology generally refers to the way in which the IP Core, NI, Router and Physical Links are connected in the NoC. The topology of the NoC is defined according to the requirements of the application. For different applications different topologies are chosen. Different topologies have different properties, and are best suited for different applications. Some of the most commonly used topologies are described below.

### I. Ring Topology

Fig 2 shows the ring topology; all the nodes are connected in a ring pattern. Regardless of the size of the network, every node has only two neighbors. The main advantage of this topology is that if faults occur they can be easily detected; but if any link breaks the entire network can be disrupted this is a major problem.

### II. Star Topology

Fig 3 shows the star topology; all the nodes are connected to a single central node. All the nodes except the central node has only one neighbour, where as the central node has (N-1) neighbours. This topology is very simple, and the average hop distance is 2. However, the failure of the central node results in the failure of the entire system.

### III. Mesh Topology

Fig 4 shows the mesh topology; all the nodes are connected in a grid pattern. Each node has 2 to 4 neighbors depending upon its position in the grid. The nodes at the edge have 2 neighbors but the nodes in the center have 4 neighbors. Adding of a new node in this topology is very easy.

### IV. Torus Topology

Fig 5 shows torus architecture; it can be obtained by modifying the existing mesh architecture by adding direct connections to two end nodes in the same row or column. The torus topology may have long links.

### V. Binary Tree Topology

Fig 6 shows the binary tree topology; the top node is called the root and the bottom node is called the leaves. Every node has two off springs. As the tree becomes big, it becomes complicated to configure.

### VI. Fat Binary Tree Topology

Fig 7 shows the fat binary tree topology; only the leaves are the IP core. There are more number of links increase by the order of 2. This topology is best suited for applications which require high degree parallelism.

### VII. Butterfly Architecture

Fig 8 shows the butterfly architecture; there is only one path from source to destination node. There are long physical links which are a major drawback.

### VIII. SPIN Architecture

Fig 9 shows the SPIN (Scalable Programmable Integrated Network); this architecture is similar to the butterfly architecture. In this topology, the router in each level consist of same number of parent port and child port.

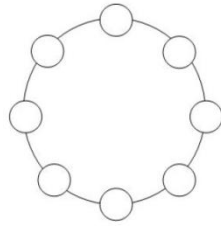


Fig. 2

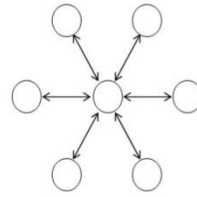


Fig. 3

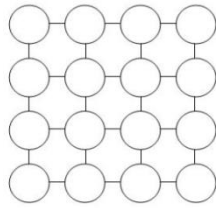


Fig. 4

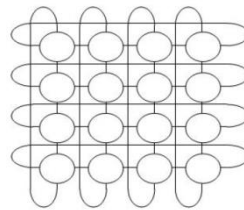


Fig. 5

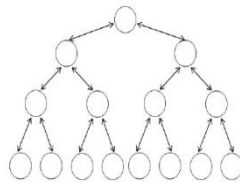


Fig. 6

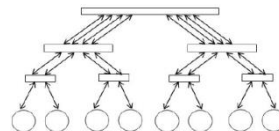


Fig. 7

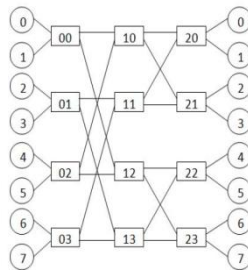


Fig. 8

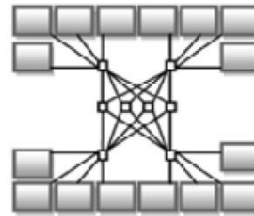


Fig. 9

### IX. Reconfigurable NoC Architecture

In the reconfigurable NoC architecture, the application running on the SoC determines the NoC configuration. The NoC architecture as viewed by the application is actually a logical topology built on the real physical topology [10]. Before the application starts the logical topology is configured according to the communication requirements in the initialization phase. This reconfiguration of topologies result in better energy, area and latency efficiency in contrast to regular topologies.

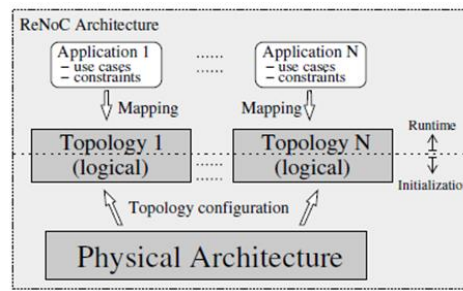


Fig. 10

The evaluation shows that the ReNoC architecture enables application-specific topologies to be configured with little overhead and indicates that the architecture has great potential for future SoC platforms[10].

### III. TOPOLOGY PARAMETER

Certain parameters are used to characterize the NoC topology. These parameters are used to distinguish one topology from another. These parameters are described below:

#### A. Node Degree

It is defined as the number of links connected to a node. If in a network all the nodes have the same node degree, the network is called regular. The Ring topology is an example of regular topology where as Star topology is irregular. A network having smaller node degree indicates that it requires less hardware cost.

#### B. Diameter

It is defined as the maximum shortest path between all pair of nodes. When the message travels through intermediate nodes a 'hop delay'. This hop delay is proportional to the number of hops. The worst case distance for broadcasting is determined by the node which is the farthest from the sender.

#### C. Link Complexity

It is defined as the total number of links in a topology. As the topology grows, the link complexity increases proportionally. By adding links in the network we can reduce the diameter. But the links may lead to added hardware complexity and area overhead.

#### D. Bisection Width

It is defined as the, number of links needed to be removed to divide the topology into two networks of approximately equal size.

### IV. PERFORMANCE METRICS

#### A. Average end-to-end Delay

It is defined as the time lapsed for a packet to travel in the network from the source to the given destination. The smaller the average end to end delay values of the delay the more efficient the network.

#### B. Loss Rate

The loss rate is defined as the ratio of the packets lost to the total number of packets generated. Low loss rate is preferable though different applications have different acceptable loss rate.

### C. Average Throughput

It is defined as the data rate (in bits/second) successfully delivered to the destination.

### V. CONCLUSION

In this paper we have discussed various NoC topologies, and we can see that the topology has a great impact on the performance of a network. From the view of high performance, low diameter and high bisection width are preferred.

But, considering the cost and effort of implementation, low degree, short wires, small area and regular structures are of great interest.

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