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SNM AND READ STABILITY ANALYSIS OF 7TSRAM CELL ON 45NM TECHNOLOGY

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Abstract: This paper explains how the noise presence in SRAM cell affects the read stability of cell. The static noise margin SNM is effectively present in SRAM cell. The SNM changes various parameters of SRAM cell. SNM varies during each cell operation. The cell ratio, pull up ratio is also playing vital role in memory cell stability. This paper has analysis how SNM varies with the threshold voltage and supply voltage.
Index Terms—*SRAM, Stability, Read margin, Write margin, SNM*

I. INTRODUCTION

The noise presence in cell affects the speed of SRAM cell and the role of supply voltage in SRAM cell for its stability and speed. In present Scenario CMOS technology has forced to work on lower to lower supply voltage so stability is main factor of CMOS SRAM cell. With enhancing technology the size of CMOS also reduced. The essential parameter of SRAM cell operation is SNM. SRAM cell depends on various types of noises and static noise margin is essential for SRAM cell speed and stability to make SRAM faster threshold on the transistor have been lowered which contribute to leakage current badly. The SRAM cell stability depends on both static and dynamic noise margin analysis. SRAM cell stability is also affected by varying the supply voltage.

II. STATIC NOISE MARGIN

Noise margin is maximum signal that can be accepted by device without data loss. SNM can be defined as maximum value of voltage that can be tolerated by the flip-flop before changing its state. The read and write margin of SRAM cell depends on SNM and also depend on threshold voltage. For increasing the speed of SRAM cell the other way is to increase the cell ratio if cell ratio increases the size of driver transistor increases due to this current increases .we got different value of SNM by changing the cell ratio. cell ratio

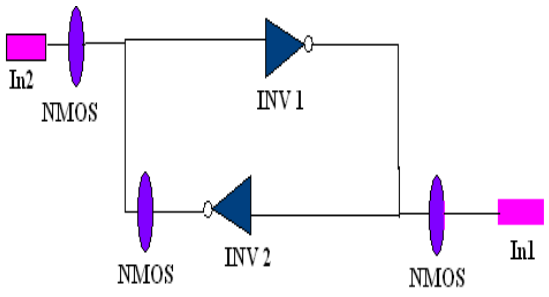

Fig.1 SRAM cell

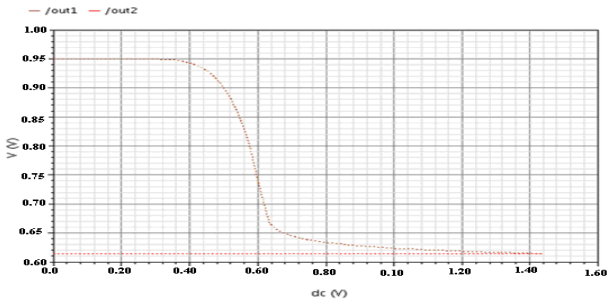

Fig.2 VTC of Inverter

SNM can also be define as side of maximum square drawn between the inverter characteristics for this approach two inverter with noise sources inserted between the input and output of SRAM cells having two noise sources applied to the input of each inverter of SRAM cell make the value of SNM to be the worst case SNM for getting best case SNM by using only one noise sources is applied or the polarities of noise sources not adverse.

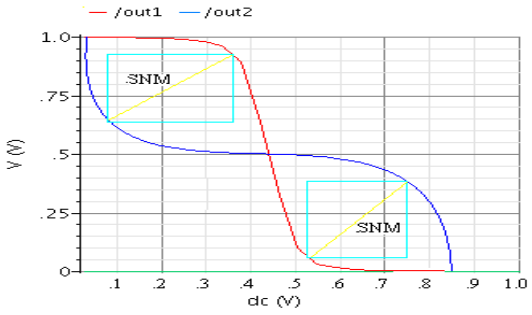

Fig.3 Butterfly Curve Measuring SNM

III. DEPENDENCE ON VDD

VDD affect the SNM of SRAM cell. VTC curve in graph shows in Fig 4 and Fig 5 shown its Transient response, How the SNM values varies with VDD for hold and read mode. In the graph the output of the inverters are shown at VDD= 1.0v and 3/4VDD = 0.75v respectively. The 180nm technology its value 1.8v and 45nm it is 1.0 volt while 32nm technology allow its lowest value. But high VDD is responsible for leakage current and other. The suitable value for 45nm technology high SNM (Cell Stability) and low leakage current is 0.9v.

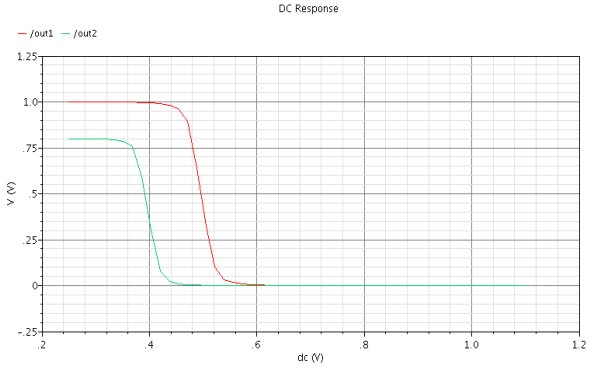

Fig.4 VTC Vs Vdd 7T SRAM Inverter

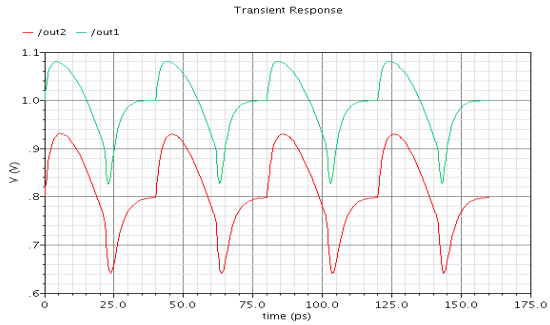

Fig.5 Transient Response of VTC Vs Vdd

IV. READ MARGIN:

Read margin of SRAM cell takes place during read operation actually read margin read stability depend on supply voltage [6]. The analysis of read margin is same as SNM it is essential while designing SRAM cell inverter firstly measure the read margin. Read margin actually read static noise margin during read operation, mainly voltages are bit. line voltage power supply voltage. During read operation the stability of cell decreases. It means during read operation the stability of SRAM cell changes Read operation is more critical it require discharging of large bit line capacitance

TABLE: 1 SNM Vs Read margin

Technology	CR	READ MARGIN	SNM
45nm	1.0	0.391	203
	1.3	0.395	205
	1.5	0.403	209
	1.7	0.407	216
	2.0	0.500	220

V. WRITE MARGIN:

The write margin is taken during write operation, Write margin variation is a function of cell design. write margin voltage is the maximum noise voltage present on bit lines during write operation[6].write margin also depend on pull up ratio as pull up ratio varied the write margin also varies .write margin is measure of the ability to write data in to the SRAM cell. The write operation is takes place when pre-charging and discharging of cell takes place precharge bit line to VDD and discharge other bit line to ground with respect to WL.

TABLE 2- SNM Vs Write margin

TECHNOLOGY	PR	WRITE MARGIN	SNM
45nm	2.8	0.472	208
	3.0	0.480	210
	3.2	0.486	214
	3.4	0.492	220
	3.6	0.497	225
	3.8	0.502	228

VI. 7T SRAM CELL STABILITY

The stability of 7T SRAM Cell depend on SNM and SNM is depend on access transistors PMOS and NMOS transistor width. The circuit of 7T SRAM cell is made of two CMOS inverters that connected to cross coupled to each other with additional NMOS Transistor which connected to read line and having two pass NMOS transistors connected to bit lines and bit-lines bar respectively. Fig 6 shows circuit of 7T SRAM Cell and Fig 7 its Layout, where the access transistors MN3 is connected to the word-line (WL) to perform the access write and MN4 is connected to the Read-line (R) to perform the read operations thought the column bit-lines (BL and BLB). Bit-lines act as I/O nodes carrying the data from SRAM cell. All transistors have minimum length while their widths are typically design parameters. The value of Wp1 and Wp2 defines PMOS transistors width and Wn1 and Wn2 defines the NMOS driver transistors width use in CMOS Invertors, while Wn3 and Wn4 is the access transistors width.

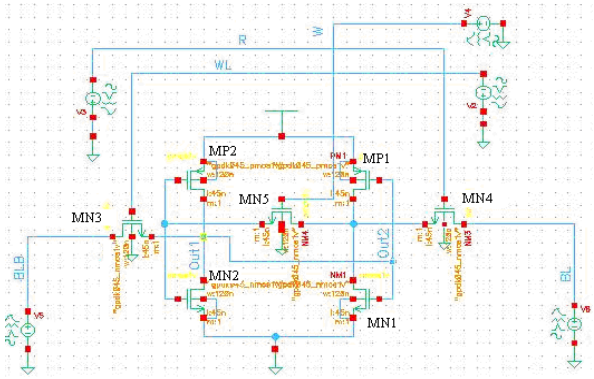

Fig.6 7T SRAM

VII. CONCLUSION

In this paper we have analysis how static noise margin (SNM) is a major parameter which effect the SRAM cell stability during various operations. We have taken write margin, read margin, supply voltage, threshold voltage analysis with SNM. The cell ratio, pull up ratio also important parameter which effect SNM also cell stability. Actually SNM is critical metric for SRAM bit cell stability this paper shows impact of different parameter on SNM

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