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Analysis of Power Dissipation and Delay in 6T and 8T SRAM Using Tanner Tool

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Abstract— Due to growth of technology scaling, at low-voltage operation, Static Random Access memory (SRAM) bit-cells suffer from large failure rate and power consumption is also more in scaling technology, In this paper we work on CMOS SRAM, To decrease the power dissipation during the Write operation because the write operation consumes more power. The charging of bit lines and discharging of bit lines dissipate more power during write "1" and write "0" operation. 8T SRAM cell includes two more transistors (NMOS) for appropriate charging and discharging the bit lines. The results of 8T SRAM cell are taken on different frequencies at power supply of 1.5 Volt. In the circuit we use the 130 nm technology, and the supply voltage of 1.5 Volt. Finally the results are compared with Conventional 6T SRAM. The power dissipated in low power 8T (transistors) SRAM cell is reduced in comparison to conventional 6T SRAM cell.

Keywords— SRAM 6T, SRAM 8T, Tanner Tool 13.0, POWER DISSIPATION, (W,S-EDIT)

I. INTRODUCTION

SRAM is mainly used for the faster memory i.e. cache memory in microprocessors, engineering workstations, mainframe computers and memory in hand held devices due to very high speed and low power consumption. The need for low-power design is becoming a big issue in high-performance digital systems such as microprocessors, Digital Signal Processing (DSP) and other applications[1]. The rapidly increasing market of mobile devices and battery powered portable electronic devices is creating demands for very small chips that consume the smallest possible amount of power. SRAM consists of almost 65% of Very Large Scale Integrated (VLSI) circuits. It is also said that memories are the biggest reason for the issue of power dissipation in any complex digital system and no digital system is complete without memories. So many techniques have been proposed to reduce the power consumption during write(0,1) operation of SRAM like, Segmented Virtual Ground Architecture for Low-Power Embedded SRAM , Low power SRAM design using half-swing pulse mode techniques and a single-bit line cross-point cell activation architecture for ultra-low power SRAM's[3]. Some other techniques which are used for low power SRAM like Half-Swing Pulse-Mode Techniques these techniques are used for reduce the power dissipation of the SRAM designed circuits[1]. All these discussed papers are used extra circuitry to reduce the power consumption. In this paper optimized SRAM cell contains two extra transistors in the pull-down path of the respective inverter to avoid charging of the bit-lines. These two transistor are controlled by an extra signal write select (WS). During read or write operation at least one of the tail(at bottom) transistor must be turned OFF to disconnect the driving path of respective inverters.

According to Karimi and Alimoradi the technology scaling in semiconductors led to undesirable consequences regarding power consumption and failure rate arise. To create a virtual power supply and a virtual ground, one PMOS transistor and one NMOS transistor can be added in series with the transistors of each logic block.

Cheng and Huang incorporate two major techniques to present architecture of a low power SRAM with quiet bit line[5]. In first to prevent the excessive full-swing on charging bit lines the authors use a one-side driving scheme for the write operation. In second, to keep all bit lines at low voltages all the times, for the read operation a precharge free pulling scheme was used by them.

II. SRAM

In order to overcome the increasing SRAM failures, SRAM structures with six, eight or ten transistors have been proposed. SRAM or Static random Access memory is a form of semiconductor (SC) memory widely used in electronics and communication (cellular phone, video camera and smart phone). It is also used in microprocessor and general computing applications. The delay during the operation read and write determine the speed of CMOS SRAM, and this is important in heigh speed applications [2].

This form of memory gains its valuable name from the fact that data is held there in a static fashion, and does not need to be dynamically updated as in the case of DYNAMIC RAM memory. The data in the SRAM memory does not need to be refreshed dynamically, it is still volatile. It means that when the power is OFF form the memory device, the data is not held, and will disappear. There are two key features of SRAM – (Static random Access Memory), and these set it out against other types of memory that are available: The data is stored statically: This means that the data is held in the semiconductor memory have no need to be refreshed as long as the power is applied to the memory. SRAM is a random access memory(RAM): A random access memory is one in which the locations in the semiconductor memory can be written to or read from in any sequence, regardless of the last memory location that was accessed. In Fig.1 , the read/write operations of an SRAM. To select a cell, the two access transistors must be "on" so that the elementary cell (flip-flop) can be connected to the internal SRAM circuitry.

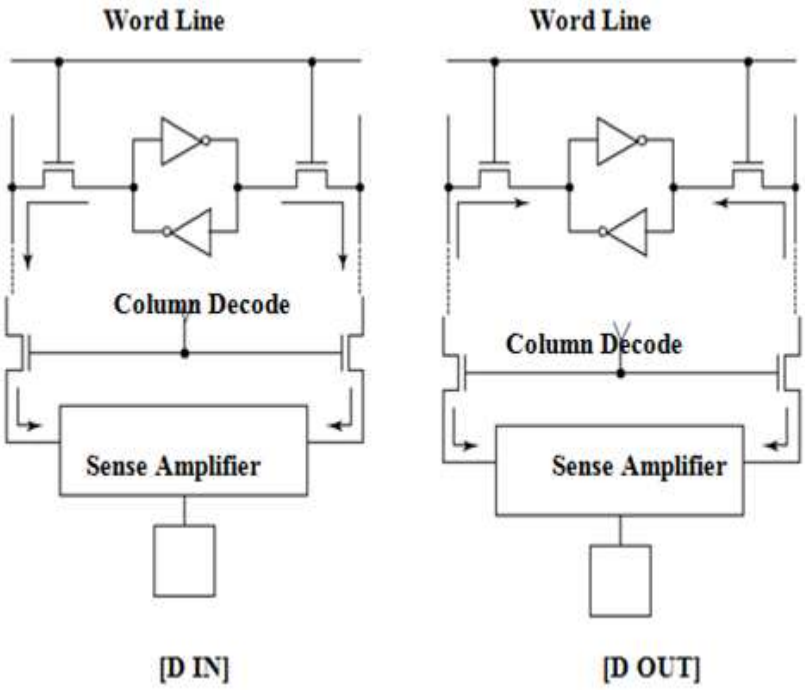

Fig. 1 Read/Write Operations

2.1 SRAM CELL OPERATION

1. Standby Mode (the circuit is idle): In standby mode word line=0, so pass transistors M3 and M4 which connect cell from bit lines are turned off and hence cell cannot be accessed. As long as the power supply is connected to the two cross coupled inverters made up of M1-M2, will continue provide feedback to each other, and the data will hold in latch [4].

2. Read Mode (the data has been requested): In read mode word line(WL)=1, as a result pass transistors M3 and M4 which connect cell from bit lines are enabled and hence cell can be accessed.

Now value stored in nodes i.e. node A & B are transferred to the BL i.e. bit line. Assume that 1 is stored at node A so BL_BAR will discharge through the transistor (M1) and the BL will be pull up through the transistors (M5 work as a load) toward VDD. Stability is required in SRAM cell so in read operation it should not be disturbed.

3. Write Mode (updating the data): Assume that we wish to change the content of the cell i.e. if previously there is a 1 and we wish to change it to a 0. To do this, the BL is lowered to 0V and BL_BAR is raised to 1V, and cell is selected by raising the WL to 1V.

III. COMPARISON ON DIFFERENT FREQUENCY (1GHz, 2GHz)

This section contains the detail simulation analysis of Low power SRAM cell for different frequencies. The dynamic power may be expressed as: $P=\alpha CV^2f$

SCHEMATIC DIAGRAM OF SRAMS (S-EDIT):

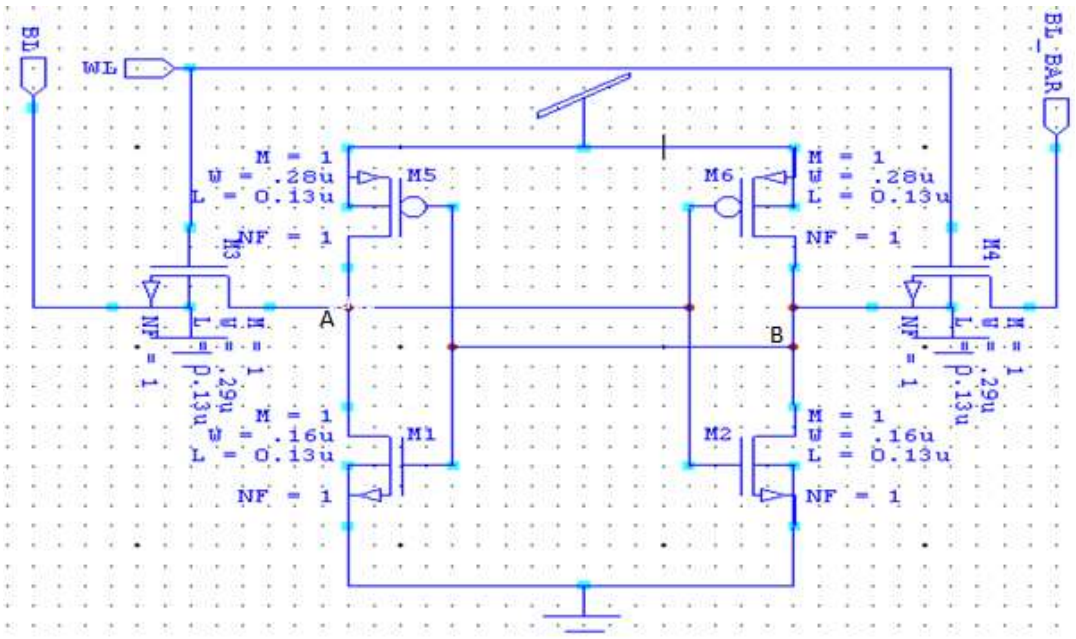

Fig. 2 Conventional 6T SRAM Cell (S-EDIT)

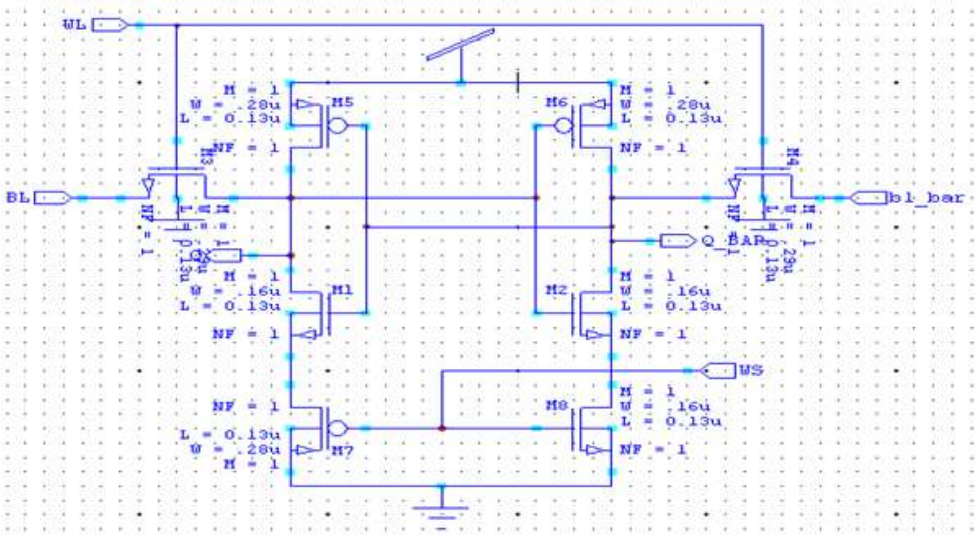

Fig. 3 Optimized 8T SRAM Cell (S-EDIT)

SIMULATION RESULTS OF SRAMS CELL AT DIFFERENT FREQUENCIES 1,2 GHz (S-EDIT):

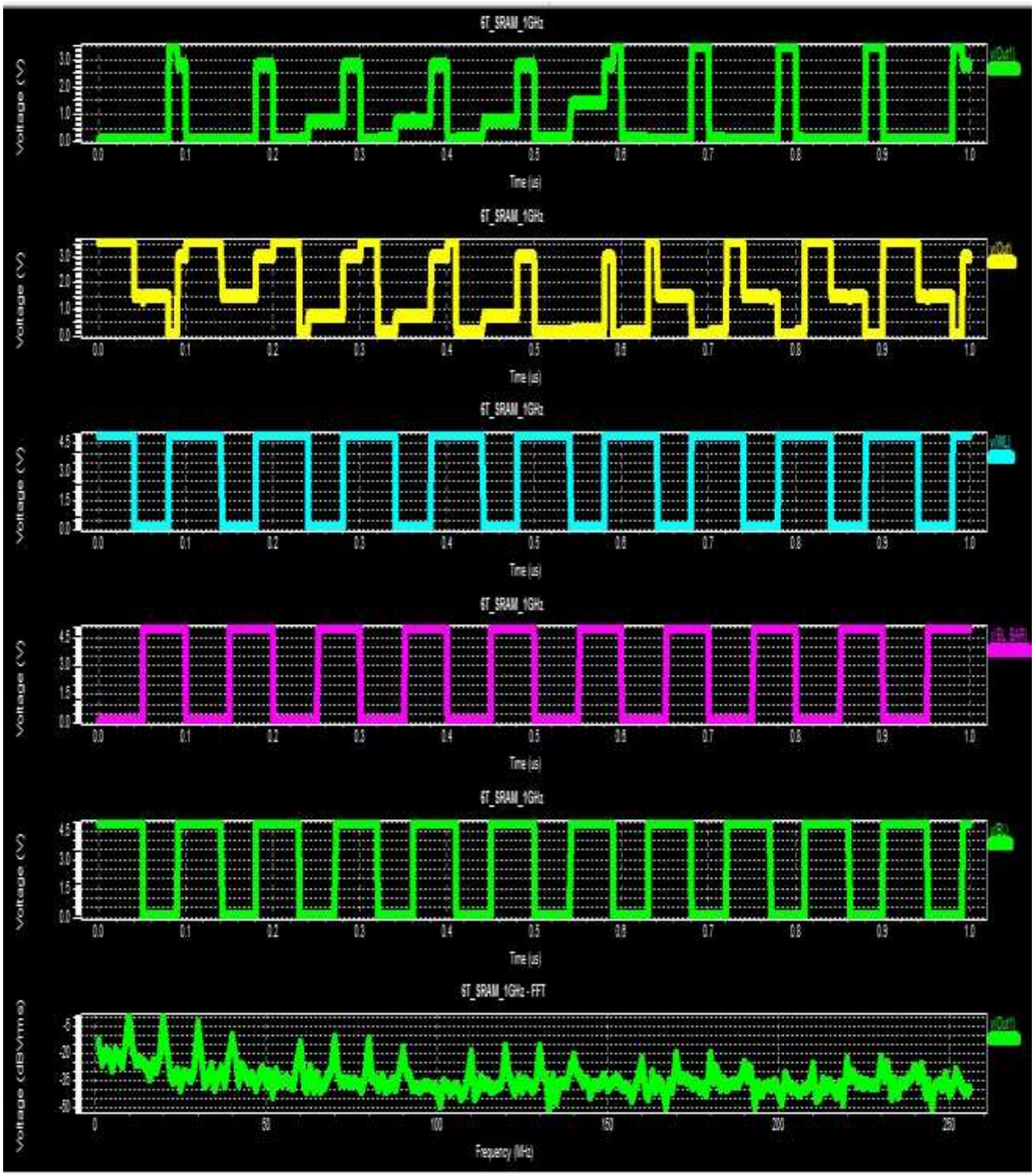

Fig. 4 Simulation Waveform of 6T SRAM at 1GHz (S-EDIT)

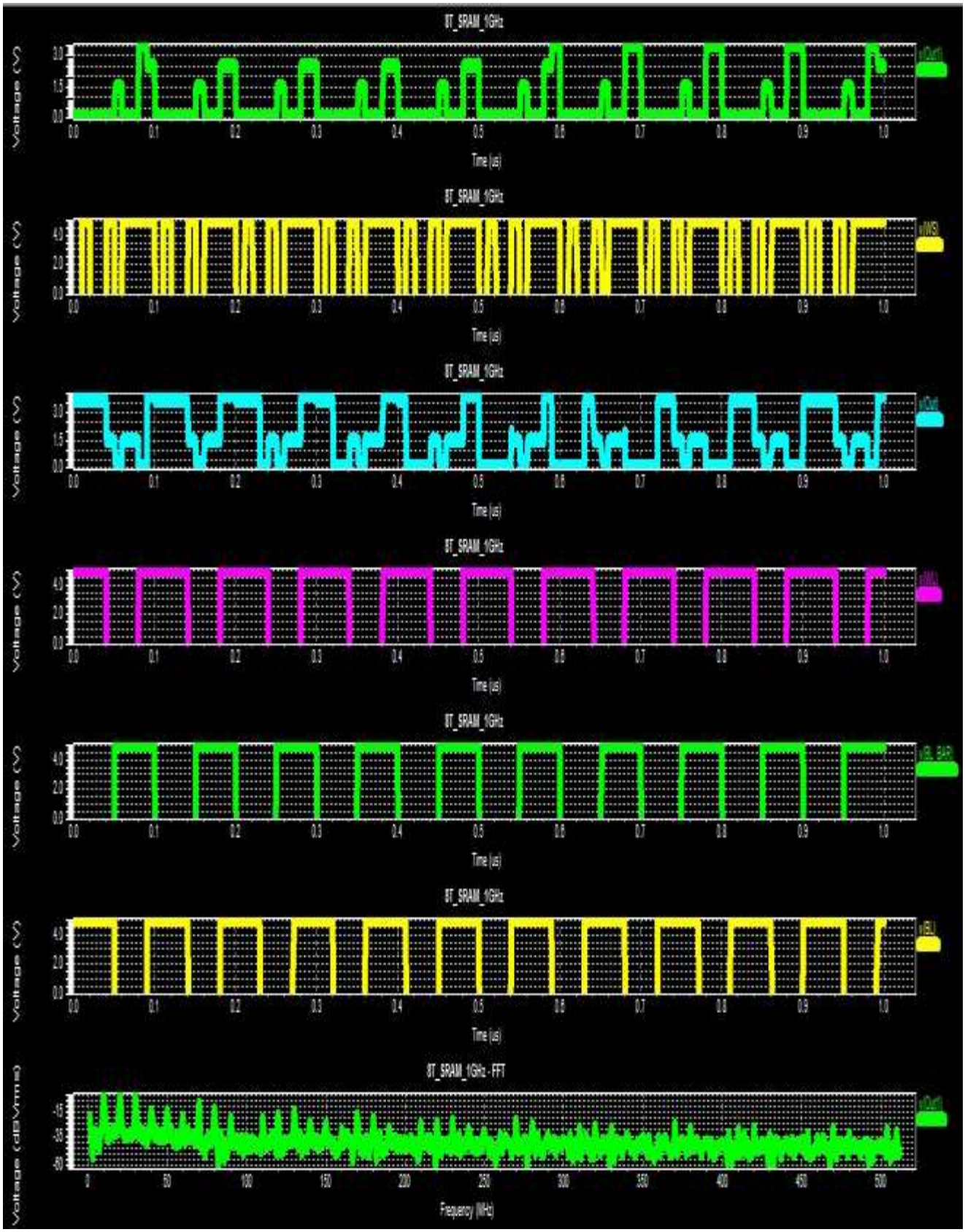

Fig. 5 Simulation Waveform of 8T SRAM at 1GHz (S-EDIT)

From the fig. 5 it clear that for frequency 1 GHz the charging time is better than discharging time, means less charging time, because of the increment in charging time and discharging time with frequency power dissipation will more.

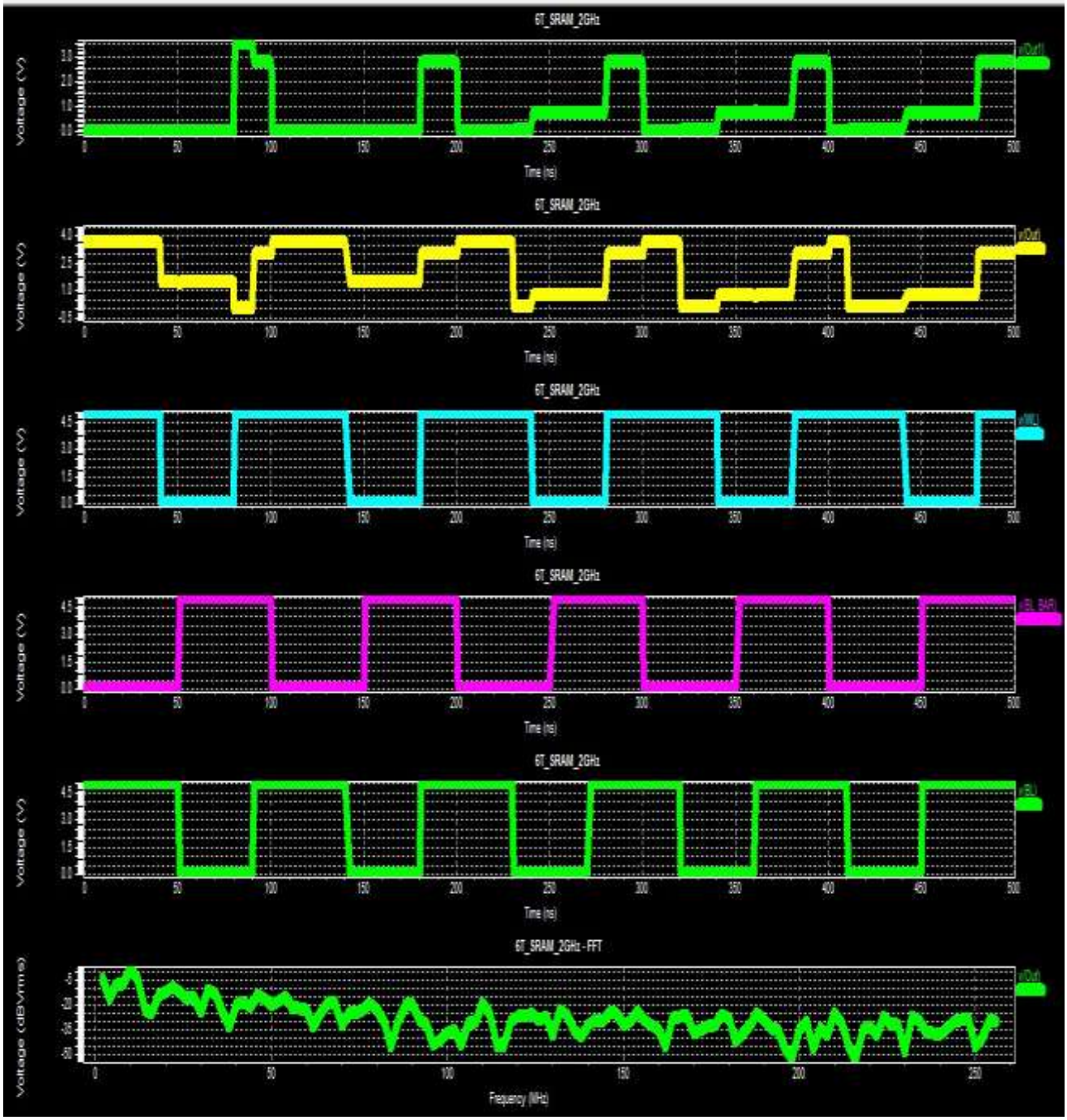

Fig. 6 Simulation Waveform of 6T SRAM at 2GHz (S-EDIT)

TABLE I.

Frequencies	Power Dissipation in 6T SRAM cell (µw)	Power Dissipation in 8T SRAM cell (µw)
1 GHz	6.75	4.72
2 GHz	9.85	8.78

In 8T SRAM cell the crosstalk voltage values are increased for bit lines, word line (WL) and comparison with conventional SRAM cell output but these values can be managed or controlled with the help of proper sizing of Width (W) and Length (L) of the transistor.

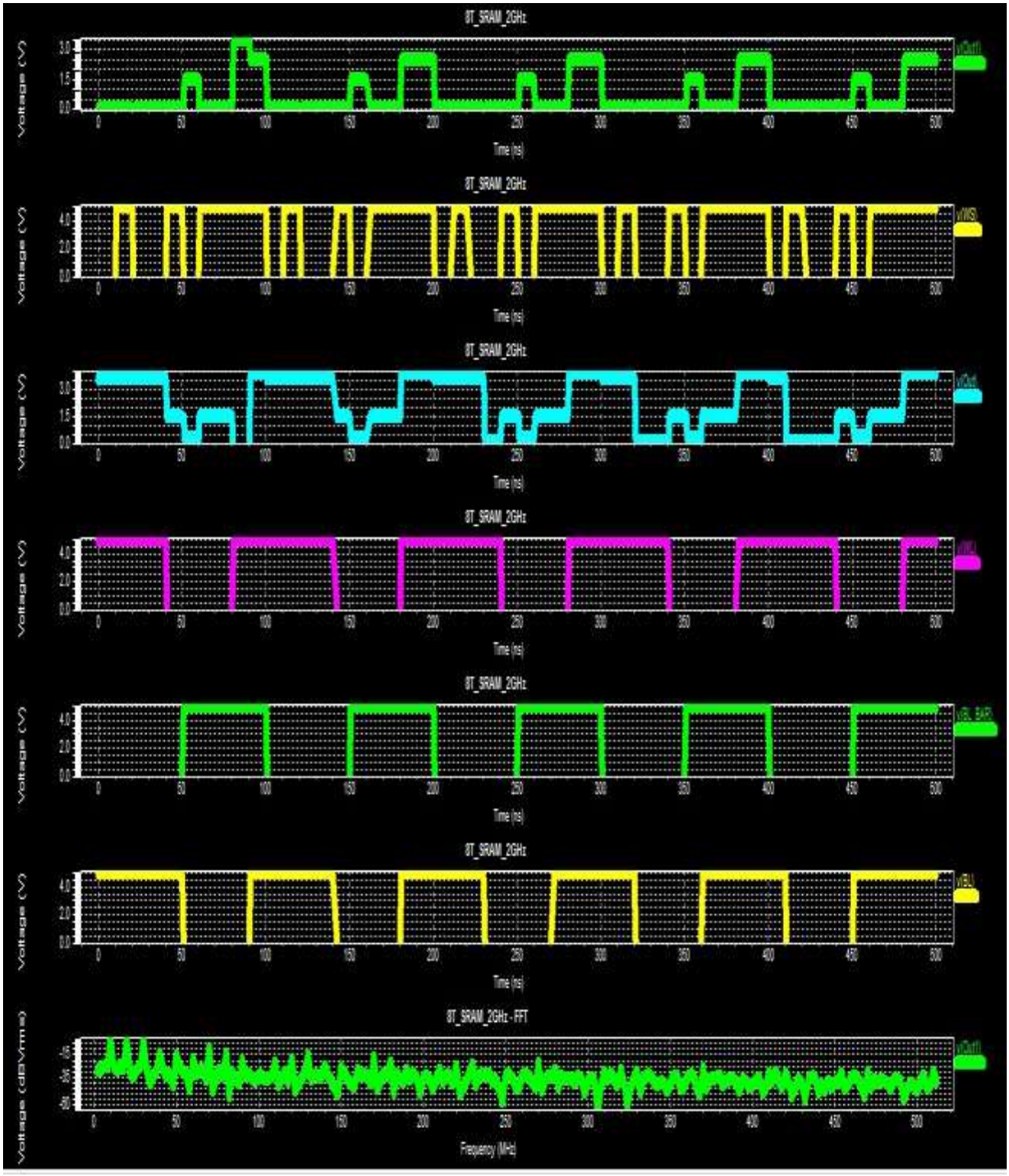

Fig. 7 Simulation Waveform of 8T SRAM at 2GHz (S-EDIT)

TABLE II.

Different SRAM Cell	Average Power Dissipation	Delay
6T SRAM	6.75 µw	5.44 ns
8T SRAM	5.52 µw	5.44 ns

In 8T SRAM cell as shown above schematic to preventing any single bit line from discharging during write "0" operation as well as write "1" operation by proper selection of WS (wire select) signal, which turn either M7 or M8 in off state .In M7 and M8 one of them is on the it will prevent from charging. The analysis of conventional 6T SRAM cell and 8T SRAM cell is shown in table II.

I V. CONCLUSION

Because of this Stack Transistors the power dissipation has reduced from 17.9 % in comparison with conventional 6T SRAM cell. The 8T SRAM provides power efficient design. There is also an improvement in the delay in 8T SRAM cell which is 28% faster as compared to the conventional SRAM cell. So the latest designed low power, low voltage SRAM cell dissipate lesser power and it has a market value in VLSI design.

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