International Journal of Recent Trends in Engineering & Research
ISSN(ONLINE) : 2455-1457
IMPACT FACTOR : 3.344

VHDL implementation of a direct digital synthesizer for various applications

Anju Narayanan[1], Mable Susan Boban[2], Parvathy S Kumar[3], Prof. Binu K Mathew[4]
[1,2,3] S8 EC Students, Department of Electronics and Communication,
SAINTGITS College of Engineering, Kottayam, Kerala
[4]Associate Professor, Dept. of Electronics and Communication Engineering,
SAINTGITS College of Engineering, Kottayam, Kerala

Abstract: - A frequency synthesizer is an electronic device which generates a range of frequency mostly sine wave from a fixed clock provided. These frequency synthesizers are commonly found in radio receivers, mobile telephones radio telephones, wacky talkies, as local oscillators, satellite receivers, GPS system. Direct digital synthesizer (DDS) is a frequency synthesizer which digitally creates arbitrary wave forms of different frequencies from the fixed frequency provided as clock input. DDS generates digital wave forms and these digital waveforms are converted to analog signals by the digital to analog converter connected at the output of DDS. The DDS designed here is a ROM based DDS. DDS has many advantages over PLL and other similar approaches such as fast settling time, sub-hertz frequency resolution, continuous phase switching response and low phase noise. This system has many applications such as the confidential message transfer, speedy frequency switching.
Index terms - Direct Digital Synthesizer, DDS, Phase Locked Loop, PLL, Digital to Analog Converter

I. INTRODUCTION

Direct digital synthesis is a method of generating analog waveforms. The wave form is first synthesized in digital form then converted into analog form using an analog to digital conversion. The wave form is generated as a digital waveform since the operations within the DDS is primarily digital. It provides fast switching between output frequencies fine frequency resolution, and operation over a broad spectrum of frequencies. Due to advances in technology DDS is very compact and draw little power.

Frequency synthesizer can be defined as an electronic device which generates a range of precise frequencies from the fixed clock provided. The expensive array of crystal resonators in a multi channel radio receiver is replaced by these types of frequency synthesizers. The crystal oscillator provides the clock frequency and the other frequencies are generated by the frequency synthesizer. These components are basically inexpensive and a digital circuitry can easily control these components. All these reasons make frequency synthesizers to be widely in included in new communication systems.

Frequency synthesizers are found in many devices such as radio receivers, mobile telephones, radio telephones, walky-talkies etc. A frequency synthesizer's function is to generate precise frequencies that are multiples of the reference frequency provided.

F (generate) = m* F(ref) /2^n

The ability to produce accurately and control waveforms of different frequencies and profile has become an important requirement common to a number of requirements. Whether providing agile sources of low-phase-noise variable-frequencies with good spurious performance for communications,

or simply generating a frequency stimulus in industrial or biomedical test equipment applications, convenience, compactness, and low cost are important design considerations. Many possibilities for frequency generation are open to a designer, ranging from phase locked loop (PLL) based techniques for very high-frequency synthesis, to dynamic programming of digital-to-analog converter (DAC) outputs to generate arbitrary waveforms at lower frequencies. In PLL based system we already need a sinusoidal signal as the input. But for DDS there is no need for sinusoidal input. The DDS technique is rapidly gaining acceptance for solving frequency or waveform generation requirements in both communications and industrial applications because single-chip IC devices can generate programmable analog output waveforms simply and with high resolution and accuracy. Furthermore, the continual improvements in both process technology and design have resulted in cost and power consumption levels that were previously unthinkably low. Direct frequency synthesizer is the oldest of the frequency synthesis methods. It synthesizes a specified frequency from one or more reference frequencies from a combination of harmonic generators, band-pass filters, dividers, and frequency mixers. The desired frequency is obtained with a filter tuned to the desired output frequency.

Direct digital synthesis (DDS) is a powerful technique which is used in the generation of radio frequency signals for use in a variety of applications from radio receivers to signals generators and many more. The technique has become far more widespread in coming few years with the advances being made in integrated circuit technology that allow much faster speeds to be handled which in turn enable higher frequency DDS chips to be made. Therefore, the output frequency is an integer multiple of the reference frequency,

$$Fo = Nfr$$

The PLL with a frequency divider in the loop thus provides a method for obtaining a large number of frequencies from a single reference frequency. In this paper, we had implemented a DDS which generates the required frequency from a reference clock. This direct digital synthesizer is a ROM based direct digital synthesizer. The sine wave amplitudes from 0 to 90 degree are stored in the ROM memory following the quarter wave symmetry of the sinusoidal signal. The sine wave is divided into four equal parts from 0 to 90 degree, from 90 to 180 degree, from 180 to 270 degree and from 270 to 360 degree. Amplitude increases from 0 to 90 degree, and 90 to 180 degree is a mirror image of the previous part. The positive half and negative half cycles are just inverse of each other. This particular DDS is designed in such a way that it generates both sine and cosine waves as cosine wave is a sine wave delayed by 90 degree.

II. LITERATURE REVIEW

Direct digital synthesis (DDS) is a technique for using digital data processing blocks as a means to generate a frequency and phase-tunable output signal referenced to a fixed-frequency precision clock source. In essence, the reference clock frequency is “divided down” in DDS architecture by the scaling factor set forth in a programmable binary tuning word. Today’s cost competitive, high performance, functionally-integrated, and small package sized DDS products are fast becoming an alternative to traditional frequency-supple analog synthesizes solutions. The integration of a high speed, high performance D/A converter and DDS architecture onto a single chip (complete DDS solution) enabled this technology to target a broader range of applications and provide, in many cases an attractive alternative to analog-based PLL synthesizers. For many applications, the DDS solution holds some distinct advantages over the equivalent agile analog frequency synthesizer employing PLL circuitry. The ability to accurately produce and control waveforms of various frequencies and profiles has become a key requirement common to a number of industries [2].

Many possibilities for frequency generation are open to a designer, ranging from phase-locked-loop (PLL) based techniques for very high frequency synthesis, to dynamic programming of digital-to-analog converter (DAC) outputs to generate arbitrary waveforms at lower frequencies. But the DDS technique is rapidly gaining acceptance for solving frequency (or waveform) generation

requirement in both communications and industrial applications because single-chip IC devices can generate programmable analog output waveforms simply and with high resolution and accuracy.

a) Principle of operation of DDS

This form of synthesis generates the waveform directly using digital techniques. The DDS technique is different to the way in which the more familiar indirect synthesizes that use a PLL as the basis of their operation. Its basic principle is to sample the phase or amplitude of a cycle of continuous sine wave with equal phase interval, get the discrete phase amplitude sequence of a periodic signal, and quantity its analog amplitude. Thus a periodic sine signal is converted into a series of discrete binary sequence, which is finally stored in a ROM memory. The content of each memory cell is the quantized amplitude of the sine wave [2]. DDS is a commanding technique used in the generation of radio frequency signals for use in a variety of applications from radio receivers to signals generators and many more. The technique has become very popular in recent years with the advances being made in integrated circuit technology that allow much faster speeds to be handled which in turn enable higher frequency DDS chips to be made. Although often used on its owned is often used in combining with indirect or phase locked loop synthesizer loops. By combining both the technologies it is possible to take the advantage of the best aspects of each. It is used for generating waveforms like sine, cosine, square etc [3], [5].

A basic Direct Digital Synthesizer consists of a frequency reference, a Numerically Controlled Oscillator (NCO), and a DAC. The reference provides a stable time base for the system and determines the frequency accuracy, stability of the DDS. It provides the clock to the NCO which produces at its output a discrete time, quantized version of the output waveform (often a sinusoidal) whose period is controlled by the digital word contained in the frequency controller register. The sampled digital waveform is converted to an analog waveform by DAC. The output reconstruction filter (LPF) rejects the spectral replicas produced by the zero-hold inherent in the digital to analog conversion mechanism[3][4].

DDS's key component is the phase accumulator. The frequency control word controls the rate of phase change. Under the control of the reference clock fs, the phase accumulator accumulates the frequency control word linearly. The summation thus adds with the phase control word, and finally forms the address to the ROM table.DDS is a new type of frequency synthesis. It directly generates variable frequency signals by controlling the rate of change in phase - a digital technology [2].

A Portable Digitally Controlled Oscillator using varactor diode is one of the works that was referred. This paper explains a portable Digitally Controlled Oscillator (DCO) using two input NOR gates as a Digitally Controlled Varactor (DCV) in fine tuning delay cell design. This novel varactor diode uses the gate capacitance difference of NOR gates under different digital control inputs to establish a DCV. The paper proposed a DCO with novel DCV can be implemented with standard cells, and thus it can be ported to different processes in short time. Phase locked loops (PLL) are widely used in many communication systems to clock and data recovery or frequency synthesis. Traditional analog circuit design such as PLL shifts the design paradigm toward more digitally intensive techniques, easier testability and less parameter variability because of process migration. However, this DCO suffers from one fundamental drawback. Due to the extremely small size of varactor, it requires intensive circuit layout and needs advanced lithography technology. A long design cycle will occur as product design transfers to different processes or the design specifications are changed. Thus, this work attempts to propose a high resolution SCO by using NOR/NAND gates as novel varactor [6].

One another work related to DDS is 'An Ultra-Low-Power and Portable Digital Controlled Oscillator for SoC applications'. In this work, a novel ultra-low-power DCO with cell based design for system-on-chip applications is presented. Based on the segmented delay line and hysteresis delay cell, the power consumption can be saved in coarse tuning and fine tuning stages, respectively as compared

with conventional approaches. Besides, the proposed DCO employs a cascade-stage structure to achieve high resolution and wide range at the same time. Large power consumption is demanded due to many DCV cells to maintain an acceptable operation range. Thus the paper attempts to propose a low power high resolution wide range DCO with high portability [7].

These two systems that were proposed were ROM-less based. Thus the next approach was a ROM based system. A Novel Rom based DDFS Architecture for Portable and Wideband communication is the existing system. The paper proposes a novel architecture for Read Only Memory (ROM) based DDFS based on simple sine trigonometric approximation formula. In the proposed architecture, to synthesize the sine wave from 0 to $\pi/2$ the sine samples from 0 to $\pi/4$ and the cosine samples from 0 to $\pi/4$, a digital multiplier, and a scaling block are used. Further the quarter wave symmetry of the sine wave is explored to derive the remaining samples that are required to synthesis the sine wave from $\pi/2$ to 2π.In the proposed DDFS architecture the sine and cosine samples are stored in two separate ROMs this saves the ROM area about 14.6% [8].The tremendous growth in modern wireless communications [9] and the rapid advancements in semiconductor IC technologies [10] have made DDFSs as an inevitable choice for frequency synthesis. The traditional communication systems are augmented with analog phase locked loop frequency synthesizers (PLLs) because of their high output frequency capabilities and high spectral purity. In spite of these advantages the analog PLLs suffer from various issues like long frequency tuning time, high phase noise, and closed loop stability and also bulky. On the other hand DDFSs offers many promising advantages such as fine frequency tuning steps in sub-hertz range, fast frequency switching times, smooth frequency transitions, ease of fabrication, low cost and low power. Thus these advantages have made them an indispensable integral part in modern high speed digital communication systems.

b) Comparison with PLL Synthesizers

The technique of direct digital synthesis (DDS) has recently become a viable alternative or complement to phase locked loop (PLL) synthesis for a wide range of applications. The DDS technique circumvents the traditional trade-offs associated with PLL architectures. Rather, a new set of trade-offs appear. Trade-offs for PLL Synthesizers includes Frequency resolution (step size), Settling time, Tuning range (bandwidth), Phase noise (spectral purity), Cost, complexity and power consumption. Trade-offs for DSS Synthesizers includes Clock speed (bandwidth), spurious responses (spectral purity), Cost, complexity and power consumption. A comparison of these two trade-offs lists implies a preference for one architecture or the other for a given application or a specific design criteria. In DDS systems the frequency resolution is determined primarily by the word length of the phase accumulator. Furthermore, in DDS systems the settling time is usually determined by the bandwidth of the alias filter. Consequently frequency resolution, settling time, and spectral purity are independent variables, unlike PLLs were they are interrelated.

c) Spectral purity in DDS systems

Phase noise for practical purposes, is not a problem in DDS systems. The digital phase number is exceedingly linear because it is produced by a stable fixed clock. This is a major advantage over PLL systems. Although phase noise is typically not an issue when discussing DDS systems, the discrete spurious signals are significant. Therefore spectral impurities in DDS systems are usually discrete narrow band spurs rather than broad band phase noise as in PLL systems. DDS offers some other interesting possibilities. The most common need of the system is quadrature generation. Before the availability of economical and high performance DDS systems the synthesizer designer was limited to PLL techniques. Today, the synthesizer designer has three options DDS, PLL, DDS + PLL. The DDS architecture is a viable architecture for many applications given to PLL designs.

III. OVERVIEW OF DIRECT DIGITAL SYNTHESIZER

Direct digital synthesizer (DDS) is basically a frequency generator. It generates the required frequency from a reference clock. This direct digital synthesizer is a ROM based direct digital synthesizer. The

wave amplitudes that have to be outputted is stored in the ROM memory. Here the sine values from 0 to 90 degree are stored, since these values form a quarter of the sine wave. The remaining parts are generated by varying the address selection. Considering a sine wave the wave can be divided into four equal parts. In those four parts from 0 to 90 degree, the amplitude is increasing and the wave during the phase interval of 90 to 180 degree is similar to the part in 0 to 90 degree only difference is that it is just the mirror image of the previous.

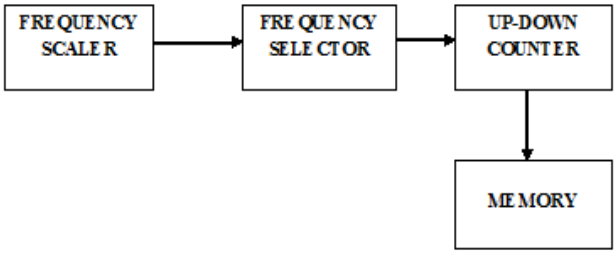

Fig.1 Block diagram of ROM address selector

The positive half and negative half cycles are just inverse of each other. This particular DDS is designed such that it generates both sine and cosine waves. The same saved amplitudes is enough to generate both sine and cosine waves. The only difference is one is 90 degree delayed than the other. Here 0.2 degree resolution is selected so 320 values are stored in the ROM memory. As the resolution is made more the wave generated will be more perfect. The resolution required is dependent on the application in which we are using it, like in digital image processing the resolution is not an important constrain. Here only 320 values are selected. Here maximum voltage is set as one volt. The amplitude can be varied according to the requirement using the DAC connected at the output of DDS. In ROM the values are stored as binary numbers. These binary numbers are of 14 bit size. The bit size is selected as 14 bit in order to increase the resolution. Mainly there are six blocks in the system, which includes Sine/Cosine selector block, Special function D flip-flops, 14-bit adder block, two's compliment block, UP-DOWN counter selector block and a two-channel 14-bit multiplexer.

The advantage of using a ROM based DDS is that it has very less delay since it is just outputting the stored value. The ROM based DDS is also less error prone since we are just outputting the stored amplitude values. In traditional PLL like frequency synthesizers the delay is more and also the chances of delay is also more. For efficient delivery of signal in case of modulations like FSK, DDS is the most adapted way. Here the DDS is designed as a function generator generating sine and cosine waves of required frequency. The frequency of the wave is varied by varying the scale factor so that the address generated can be varied (for example if we are inputting the scale factor as '2' then the amplitudes stored in the locations 0, 2, 4, 6, 8 etc) there by reducing the time period thus increasing the frequency. The only inputs that have to be provided to this DDS are the clock, reset input and scale factor. Reset is provided here to do the sine or cosine selection. As the delay is minimized by this DDS, the efficient transmission of the message is ensured. Dividing the frequency of the common clock the frequency that the user requires is generated.

$$T_{wav} = (T_{osc} * 640) / \text{scale factor}$$

The above equation gives the time period of the wave generated by this particular DDS. In this DDS, delay is minimal as computational delay is not present inside this DDS. Aging is not a major problem regarding this DDS. Since no mechanical parts for tuning is used. So it is suitable for long time use and suitable for the communication purpose in confidential message transmission like military applications. The major disadvantage is the frequency range that can be achieved. As we have stored 320 amplitude values only, the factors of 320 can only be inputted as the scale factor. Another

disadvantage is that only increase of frequency is possible here. When the ROM size increases a FPGA having that much number of MUXs has to be selected to implement this DDS. DDS include two major blocks ROM_ADDRESS_SELECTOR and ROM VALUE SELECTOR. The working of this DDS can be simply explained as selection of the stored wave amplitude values according to the common clock provided. For the same purpose a memory and the address generator of the memory is required. So it can be said that the main parts of the DDS are a counter and a memory. The ROM_ADDRESS_SELECTOR which is 14 bit wide acts as the address of the memory location where the values are stored and the scale factor is entered at run-time by the user. When the scale factor is varied the count interval is varied, which causes the ROM addresses generated to be varied. Any variation in the count interval varies the selection of the stored amplitude value. This helps to obtain various range of frequency that should be generated as needed by the user. The counter is a Bidirectional counter and the up and down counting is controlled by the counter output itself. The down counting is carried out by adding the compliment value of scale factor to the counter output. The counting is controlled such that for the sine wave the counting starts from the initial address position (ROM address=0) and for cosine waves the counting starts from the final address position (ROM address value=320). The three inputs of the ROM_ADDRESS_SELECTOR are Clock, Reset and Scale factor. The counting is done such that on up counting the quarter of the wave is generated and on down counting the remaining quarter of the wave is generated, since one quarter of the wave is a mirror image of the other. Thus one half of the wave is generated and the other half of the wave is generated by inversing the half wave generated which is done by complimenting the value stored in ROM. The sine wave is a 90 degree delayed cosine wave, which is utilized for the generation of cosine wave. The counting is started from the final value then decrements in order to generate the cosine wave, since cos(0) is '1'. The flip-flop (DDS_DFF_SINCOS_SELECT) is having to resets, one to output the cosine wave values and other to output the sine wave values. When the reset input is “01” then we get sine wave output and when the reset input is “10” then we get cosine wave output. The maximum count of this counter is set as 320, as the maximum ROM address value is 320. Basically the counter consists of two major parts - a 14 bit ripple carry adder and a flip-flop. Since we need bidirectional counting, the counter output is complimented to get the down counting. The UPDOWN_COUNT_SELECTOR block selects the real count or complimented count based on the logic value at the MUX selection line.

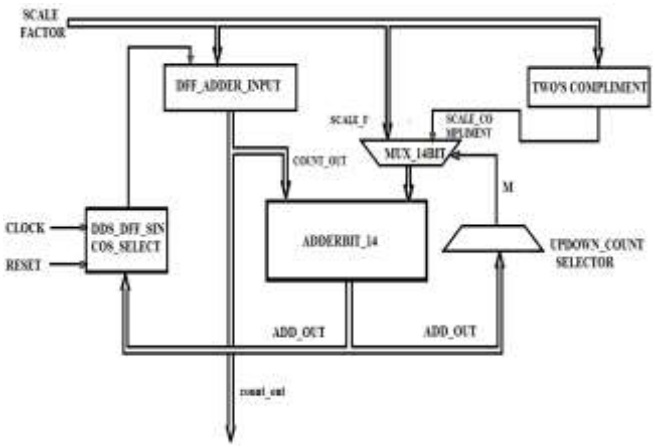

Fig. 2 Block diagram of ROM_VALUE_SELECTOR

Fig. 2 shows the block diagram of the block, ROM_VALUE_SELECTOR which selects various values from ROM memory. This block is the combination of both ROM memory and ROM_ADDRESS SELECTOR. Inside the ROM memory, three hundred and twenty values at 0.2 degree resolution are stored to construct one quarter of a sine wave. These values are selected

according to the clock input. The flip flop at the ripple carry adder input is used to control the values inputted to the adder. The common reference clock frequency is divided by the scaling factor helps to give the frequency required by the user. Since sine and cos are the two waves that only differ in the delay between them, sine and cosine waves can be generated using same set of values stored in the ROM memory. Inside the ROM the sine values are stored in the consecutive locations from 0 degree to 90 degree. Here the angle or phase values become the address locations and the amplitude values to be the data stored in the ROM memory. Both the address and data line are of 14 bit size. The ROM address selector is used to select the amplitude values stored inside the ROM memory. The values directly outputted during UP COUNT will help to generate only a quarter of the wave and second quarter of the wave is generated during DOWN COUNT of the counter. Remaining part of the sine wave is generated by complimenting the ROM output. The stored amplitude values and the complimented amplitude values are applied to a MUX and the MUX selection line is controlled by the ROM output itself for this purpose the block cycle_selector is introduced.

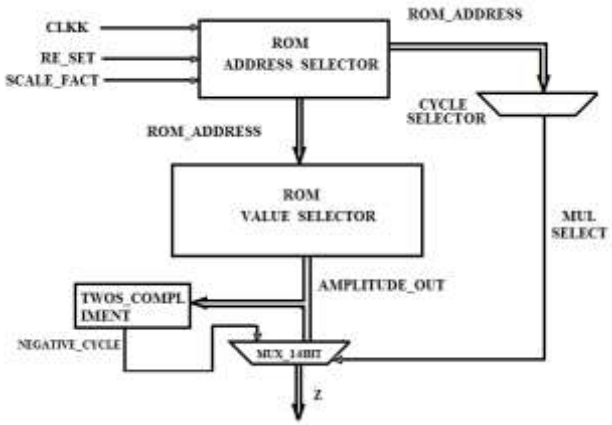

Fig. 3 Amplitude selection for various values of angles

IV. EXPERIMENTAL RESULTS

The DDS block coding is done in VHDL and simulation is done using Modelsim5.4e. The waveforms are shown in Fig. 4 and Fig.5. The code is synthesized using Xilinx ISE and downloaded into the FPGA. Amplitude values for sine and cosine signals are stored in rom. It generates the required frequency from a reference clock. The same saved amplitudes is enough to generate both sine and cos waves. The only difference is one is 90 degree delayed than the other. Here 0.2 degree resolution is selected so 320 values are stored in the ROM memory. As the resolution is made more the wave generated will be more perfect. The resolution required is dependent on the application in which we are using it, like in digital image processing the resolution is not an important constrain

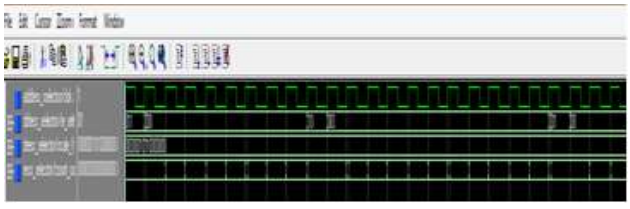

Fig. 4 Waveforms of the proposed DDS system

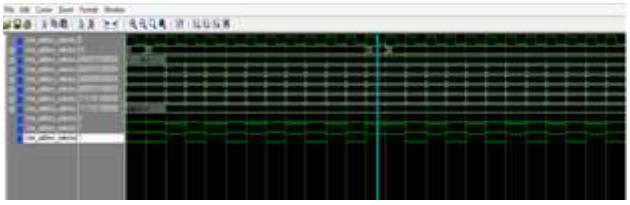

Fig. 5 Waveforms of the proposed DDS system

V. CONCLUSION

DDS can be considered as a proved efficient frequency synthesizer having various applications. It has various advantages such as the problem of aging is not affected, frequency tuning without delay is also possible. The ROM based DDS is reliable technology in the applications in which the message delivery is an important aspect like in military services. Since it has minimum delay the loss of message caused at the receiver of a communication system during tuning of the local oscillator can be minimized by replacing the local oscillator by DDS. Quarter wave symmetry is used which reduces the delay. Sine and cosine wave selection possible. Since no mathematical calculation is done just stored values are outputted so delay is minimized up to a large limit.

REFERENCES

1. An Improved Analog Waveforms Generation Technique using Direct Digital Synthesizer Gaurav Gupta and Monika Kapoor, Dept. of Electronics and Telecommunication Engineering Lakshmi Naraian College of Technology, Bhopal, M.P., India
2. Fang Yi-yuan, Chen Xue-jun, "Design and simulation of DDS based on Quartus II" .Copmuter Science and Automation Engineering (CSAE), 2011 IEEE international conference on June 2011: 357-360.
3. Manoj Kollam, S.A.S.KrishnaChaithanya, Nagarajukommu, "Design and Implementation of an Enhanced DDS Based Digital Modulator For Multiple Modulation Schemes" International Journal of Smart Sensors and Ad Hoc Networks (IJSSAN), Volume-1, Issue-1, 2011.
4. Wenmiao Song, Qiongqiong Yao. "Design and Implementation of QPSK Modem Based on FPGA" Computer Science and Information Technology (ICCSIT), 2010 3rd IEEE international conference on July 2010: 599-601.
5. Zhong Wei-jie, JIANG Lei, LIU Yao-ying. "Design of DDS Based on VHDL Editing Routine", Shipboard Electronic Countermeasure .2007, 30(2):102-105.
6. A Portable Digitally Controlled Oscillator Using Novel Varactors Pao-Lung Chen, Ching-Che Chung, and Chen- Yi Lee
7. An Ultra-Low-Power and Portable Digitally Controlled Oscillator for SoC Applications Duo Sheng, *Student Member*, *IEEE*, Ching-CheChung, *Member*, *IEEE*, and Chen-Yi Lee, *Member*, *IEEE*
8. A Novel ROM based DDFS Architecture for Portable and wide band Communication Parameshwara M. C* and Srinivasaiah H. C+
9. F. Akyildiz, David M. Gutierrez-Estevez, and Elias Chavarria Reyes, ―The evolution to 4G cellular systems: LTE-Advanced,‖ Elsevier Journal of Physical Communication, pp. 217- 244, 2010.
10. 2013PIDS_Summary.pdf, available at http://www.itrs.net/ITRS.

