Enhanced Ground Bounce Noise Reduction In a Low Leakage 0.7 Volt CMOS Full Adder Cell

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Abstract: Multi-threshold CMOS (MTCMOS) technology is an effective sub-threshold leakage power reduction method in CMOS circuits, which satisfies high-performance and low-power design requirements. The optimization of virtual supply network plays an important role in MTCMOS low-power design. In modern high performance systems-on-chips (SoCs), more than 40% of the total active mode energy can be dissipated due to the leakage currents [1]. With more transistors integrated on-die, leakage currents will soon dominate the total energy consumption of high performance SoCs. Furthermore, leakage current is the only source of energy consumption in an idle circuit. The battery-powered portable systems such as cell phones and laptop computers tend to have long standby modes. Reducing the leakage energy consumption of the portable systems during these long idle periods is crucial for a longer battery lifetime. This paper is based on leakage current and active power reduction in 10 transistor pass transistor based single bit full adder using MTCMOS techniques for 45nm scale using cadence tool. A 20 ns access time and frequency 0.05 GHz provide 45 nm CMOS process technology with 0.7 V power supply is employed to carry out 1-bit Full Adder.

Key words — Low power, MTCMOS, Tri-mode MTCMOS, Forward body bias MTCMOS, Full adder, Leakage current, Mode transition noise.

I. INTRODUCTION

The extensive development in the field of portable systems and cellular networks has intensified the research efforts in low power microelectronics. The low-power design has become a major design consideration. The design criterion of a full adder cell is usually multi-fold. Transistor count is, of course, a primary concern which largely affects the design complexity of many function units such as multiplier and algorithmic logic unit (ALU). The limited power supply capability of present battery technology has made power consumption an important figure in portable devices. The speed of the design is limited by size of the transistors, parasitic capacitance and delay in the critical path. The driving capability of a full adder is very important, because, full adders are mostly used in cascade configuration, where the output of one provides the input for other. If the full adders lack driving capability then it requires additional buffer, which consequently increases the power dissipation. In the last decade, the full adder has gone through substantial improvement in power consumption, speed and size, but at the cost of weak driving capability and reduced voltage swing. However, reduced voltage swing has the advantage of lower power consumption [1,2]. There is no ideal full adder cell that can be used in all types of applications [3]. Hence novel architectures such as CMOS, Transmission Gate (TG), Pass-Transistor Logic (PTL), Complementary Pass-transistor Logic (CPL) [5] and Gate Diffusion Input (GDI) are proposed to meet the requirements. Each design style has its own share of advantages and disadvantages. Gate Diffusion Input is a low power design that reduces transistor count. But the major problem of GDI is that it requires twin well CMOS or silicon on insulator (SOI) process for fabrication [4]. Thus GDI chips are more expensive. These logic styles and their combinations (Hybrid) are commonly used in designing full adder cells. In this paper, we have given a brief description of the evolution of full adder circuits in terms of lesser power consumption, we have used 10-transistor pass transistor based single bit full adder and computed
leakage current and active power for it. Then MTCMOS, Tri-MTCMOS and Forward body bias MTCMOS techniques are used and comparative analysis of leakage current reduction and active power reduction is done over these techniques.

II. ADDERS

2.1 One Bit Full Adders

A one-bit full adder is a combinational circuit that performs the arithmetic sum of three bits. It consists of three inputs a, b and cin and two outputs S and Cout as show in figure. (1)

\[
S = A \oplus B \oplus C_i = A \overline{B} \overline{C_i} + \overline{A} B \overline{C_i} + \overline{A} B C_i \ldots \ldots 3 \\
C_o = AB + (A + B)C_i \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots 4
\]

2.2 RIPPLE CARRY ADDER

A simple ripple carry adder is a digital circuit that produces the arithmetic sum of two binary numbers. It can be constructed with full adders connected in cascade, with the carry output from each full adder connected to the carry input of the next full adder in the chain. Figure 2 shows the interconnection of four full adder (FA) circuits to provide a 4-bit ripple carry adder. Notice from Figure 2 that the input is from the right side because the first cell traditionally represents the least significant bit (LSB). Bits a0 and b0 in the figure represent the least significant bits of the numbers to be added. The sum output is represented by the bits s0-s3. The main problem with this type of adder is the delays needed to produce the carry out signal and the most significant bits. These delays increase with the increase in the number of bits to be added.

\[
\begin{align*}
S_i &= (a_i \oplus b_i) \oplus c_i \\
C_{i+1} &= a_i b_i + (a_i \overline{b_i}) c_i 
\end{align*}
\]

2.3 CARRY LOOKAHEAD ADDER (CLA)

The carry look ahead adder (CLA) solves the carry delay problem by calculating the carry signals in advance, based on the input signals. It is based on the fact that a carry signal will be generated in two cases:

1. When both bits a_i and b_i are 1, or
2. When one of the two bits is 1 and the carry-in is 1. Thus, one can write,

\[
\begin{align*}
C_{i+1} &= a_i b_i + (a_i \overline{b_i}) c_i \\
S_i &= (a_i \oplus b_i) \oplus c_i
\end{align*}
\]
III. DESIGNING TECHNIQUES

3.1 Pass Transistor Logic

In electronic design, pass transistor logic (PTL) describes several logic families used in the design of integrated circuits. It reduces the count of transistors used to make different logic gates, by eliminating redundant transistors. Transistors are used as switches to pass logic levels between nodes of a circuit, instead of as switches connected directly to supply voltages. This reduces the number of active devices, but has the disadvantage that the difference of the voltage between high and low logic levels decreases at each stage. Each transistor in series is less saturated at its output than at its input. If several devices are chained in series in a logic path, a conventionally constructed gate may be required to restore the signal voltage to the full value. By contrast, conventional CMOS logic switches transistors so the output connects to one of the power supply rails, so logic voltage levels in a sequential chain do not decrease. Since there is less isolation between input signals and outputs, designers must take care to assess the effects of unintentional paths within the circuit. For proper operation, design rules restrict the arrangement of circuits, so that sneak paths, charge sharing, and slow switching can be avoided. Schematic diagram of 10 transistor structured pass transistor based single bit full adder is shown in figure below.
Figure-5 shows the transient input-output response of 10 transistor full adder. As clear from the figure that input-output combinations satisfy full adder functionality. Leakage current and Active power computation for this is shown below.

**Figure. 6 Leakage current waveform for 10 transistor full adder**

### IV. MTCMOS

Multi-threshold voltage CMOS (MTCMOS) is one of the most commonly used leakage power suppression techniques. The multi threshold CMOS technology has two main features. First, “active” and “sleep” operational modes are associated with MTCMOS technology, for efficient power management. Second, two different threshold voltages are used for N channel and P channel MOSFET in a single chip [5]. This technique based on disconnecting the low threshold voltage (low-Vt) logic gates from the power supply and the ground line via cut-off high threshold voltage (high-Vt) sleep transistors is also known as “power gating.” When a conventional MTCMOS circuit transitions from SLEEP mode to ACTIVE mode, high instantaneous currents flow through the sleep transistors. Large voltage fluctuations occur on the power and ground distribution networks. Noise generated in one power-gating domain during a wake-up event is transferred through the shared power and ground distribution networks to the surrounding active circuit blocks. The logic states of active circuit blocks are thereby disturbed in a multi-domain MTCMOS circuit. Here we apply MTCMOS technique on 1-bit Full Adder in which we use a high Vth PMOS transistor connected to the V_{dc} terminal of 1-bit Full Adder and a high Vth NMOS transistor is connected to the ground terminal of 1-bit Full Adder. MTCMOS is a variation of CMOS chip technology which has transistors with multiple threshold voltage (Vth) in order to optimize delay or power. The Vth of a MOSFET is the gate voltage where an inversion layer forms at interface between insulating layer (oxide) and the substrate (body) of the transistor. Low Vth devices switch faster, and are therefore useful on critical delay paths to minimize clock period. The penalty is that low Vth devices have substantially higher static leakage power. High Vth devices are used on non-critical path to reduce static leakage power without incurring the delay penalty. Typical high Vth devices reduce the static noise by 10 times compared with low Vth devices.

The schematic diagram of MTCMOS full adder and its input & output waveform is shown in figure below.

**Figure. 7 MTCMOS Full adder**
In this section, we design our circuit with Forward Body Biased MTCMOS technique for leakage current and Ground Bounce Noise reduction. In this technique high threshold transistors $N_1$, $N_2$ and $P_1$ are used to reduce standby leakage current effectively. Transistors stacking $N_1$ and $N_2$ is used to reduce leakage current in standby mode. An additional wait mode is introduced between sleep and active mode. So that discharging of ground voltage during sleep-to-active mode is divided into two parts: sleep-to-wait and wait-to-active mode. Capacitor $C_2$ has been used in order to control the drain current flowing through the transistor $N_2$. Forward Body Biasing voltage ($V_{BIAS}$) has been applied to voltage can reduce and more ground voltage is discharging during sleep-to-wait mode transition.

In standby mode sleep transistor $N_1$, $N_2$ and $P_1$ are turned OFF. The sub-threshold leakage current is shown below

$$I_{SUB} = Ae^{rac{q}{nkT}}(V_{GS} - V_{TH} + \gamma V_{BS} + \eta V_{DS}) \left(1 - e^{-\frac{qV_{DS}}{kT}}\right)$$

And
\[ A = \mu_n C_{OX} \frac{W}{L} \left( \frac{KT}{q} \right)^2 e^{1.8} \]

Where, \( V_{TH} \) = threshold voltage, \( \gamma \) = body effect coefficient, \( \eta \) = DIBL coefficient, \( C_{OX} \) = Gate-Oxide capacitance, \( \mu_n \) = mobility, \( V_{GS} \) = gate-to-source voltage, \( V_{BS} \) = bulk-to-source voltage, \( V_{DS} \) = drain-to-source voltage. When sleep transistors (N_1, N_2 and P_1) are turned OFF in standby mode then the drain-to-source potential (\( V_{DS1} \)) of N_1 decreases, which results in less drain induced barrier lowering and negative body-to-source (\( V_{BS1} \)) of N_1 causing more body effect. In this way these stacking transistors are reduced the leakage current.

Ground bounce noise is reduced by controlling the current surge flowing through sleep transistor during sleep-to-active mode transition. In mode transition there are two parts: sleep-to-wait transition and wait-to-active mode transition. During first transition (sleep-to-wait), transistor P_1 turned ON and transistors N_1 and N_2 are turned OFF. By using voltage source (\( V_{BIAS} \)) we will decrease the threshold voltage of sleep transistor, so more virtual ground can discharge during wait mode. In second transition (wait-to-active), transistor P_1 turned OFF and transistor N_1 and N_2 are turned ON. First transistor N_1 turns ON and after some delay (\( \Delta T \)) transistor N_2 will ON. \( R_1 \) is the ON resistance of transistor N_1, \( C_1 \) is internal capacitance at virtual ground (\( V_{GND1} \)) and \( C_2 \) is external capacitance at intermediate node (\( V_{GND2} \)). Capacitor \( C_1 \) having voltage \( V_1 \) and capacitor \( C_2 \) has voltage \( V_2 \). When \( 0 < T < \Delta T \), \( C_1 \) will start discharge and capacitor \( C_2 \) start charging. This process continuously until both capacitors (\( C_1 \) and \( C_2 \)) has same potential. So, if we control capacitor \( C_2 \) and delay (\( \Delta T \)), intermediate node voltage can be controlled and both the transistors are turned ON in triode region and hence, voltage fluctuation is controlled at ground and ground bounce noise will reduce.

Single bit full adder with this scheme is shown below with leakage current and active power computations.
VI. DELAY OF FULL ADDER CELL

Delay of a cell depends on input transition and output load. We have calculated the delay of full adder cell using Mtcmos & Trimode & Forward Body Bias Technique[6]. In case of MTCMOS 1 Bit full adder the values of delays for Sum and Carry are 1.22ns and 1.78ns respectively. And when we have applied the Trimode Mtcmos on 10 Transistor CMOS full adder cell then the number of transistor are increased, so the value of delays are increased i.e.3.94ns & 2.35ns and for Forward Body Bias the number are increased so the value of delay is 8.93ns & 9.14ns for sum and carry operation.
VII. CONCLUSION

Among different MTCMOS techniques presented in this chapter MTCMOS based Forward Body Bias is identified as most preferable technique because of smaller peak of ground noise, standby leakage current. Forward body biasing in FBB multimode based MTCMOS technique compensates increased delay which comes into picture because of additional transistors as compared to trimode MTCMOS technique. Use of transistor stacking, forward body biasing reduces ground bounce noise and standby leakage current with considerable amount. Low Vth devices switch faster and are therefore useful on critical delay paths to minimize clock period. The penalty is that low Vth devices have substantially higher static leakage power. High Vth devices are used on non-critical path to reduce static leakage power without incurring the delay penalty. Typical high Vth devices reduce the static power by 10 times compared with low Vth devices. Comparison analysis of different MTCMOS techniques in term of ground bounce noise, standby leakage current, active power and delay.

REFERENCES