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TLA FOR PREEMPTIVE SCHEDULING

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Abstract: These designs pose significant challenges to the channel management scheme, flow, and tools. This paper introduces several test logic architectures that facilitate preemptive test scheduling for SC circuits with embedded deterministic test-based test data compression. The same solutions allow efficient handling of physical constraints in realistic applications. This paper presents several techniques employed to resolve problems surfacing when applying scan bandwidth management to large industrial multicore system-on-chip (SC) designs with embedded test data compression. A detailed case study is illustrated herein with a variety of experiments allowing one to learn how to tradeoff different architectures and test-related factors. Finally, state-of-the-art SC test scheduling algorithms are architected accordingly by making provisions for: setting up time-effective test configurations; optimization of SC pin partitions; allocation of core-level channels based on scan data volume; and more flexible core-wise usage of automatic test equipment channel resources.

Keywords*:* Bandwidth management, scan-based test, Test Logic Architectures (TLA), test application time, test compression, test scheduling.

I. INTRODUCTION

The approach presented includes: a solver able to using input and output channels dynamically test scheduling calculations and TAM design schemes, all devised for that embedded deterministic test (EDT) atmosphere. This trend has boosted the growing recognition of system-on-nick (SC) designs due to remarkable ability to encapsulate many disparate kinds of complex IP cores running at different clock rates with various power needs and multiple power-supply current levels. Today's multicore nick architectures require no trivial test solutions enforced through the relentless miniaturization of semiconductor products, that have become considerably faster and fewer power hungry than their forerunners. Many SC-based test schemes suggested to date utilize devoted instrumentation, including test access systems (TAMs) and test wrappers TAMs are usually accustomed to transfer test data between your SC pins and embedded cores, whereas test wrappers make up the interface between your core and SC atmosphere. Packet-switched systems-on-nick can replace devoted TAMs in testing of SC by delivering test data with an on-nick communication infrastructure [1]. You will find techniques addressing synergistically TAM and wrapper design in addition to test data compression ATE funnel bandwidth management for SC designs can enjoy a vital role in growing test data compression without any visible effect on test application time. The assumption is that cores within the SC are generally heterogeneous modules, or wrapped testable models, and they have their individual EDT-based compression logic, that is subsequently interfaced with ATE with an enhanced quantity of channels. Consequently, test scheduling and TAMs can assign a small fraction of the ATE interface ability to each core. Zinc heightens compression ratios and enables tradeoffs between your test application time, amount of test data, test pin count, and interface design complexity. The plan of is relevant to the SC-based test data reduction plan able to work having a different quantity of in and output channels.

Applying a hierarchical DFT methodology for designs with a lot of cores poses significant challenges. To begin with, the amount of nick-level pins is restricted and doesn't suffice they are driving all cores in parallel. Because of the pin restrictions, it's impossible to look for the optimal allocation of pins to cores to find the best compression. In addition, since a specific core could be reused in multiple designs, an ideal quantity of funnel pins with this core when baked into one design may invalidate test reuse in other kinds. Under such conditions, the nick integrators collect data for those individual cores, check out the data together with all constraints for that design, after which by hand determine test schedules. This may lead to suboptimal test data volume and compromised test application time, especially due to some outlier blocks getting large pattern counts (Computers). Bandwidth management mitigates the dependence of core channels on the amount of available nick-level pins, enables automatic scheduling of tests by looking into making it transparent towards the customers, and considerably improves test planning in the core level. Additionally, it arbitrates the discussing from the nick-level funnel pins, therefore guaranteeing the very best data volume and test time reductions in price for the general design. Within this paper, we present a bandwidth management plan for hierarchical designs that allows an artist compromise fixed and versatile funnel allocations per core in addition to physical constraints to reduce the routing overhead from the TAM-based systems.

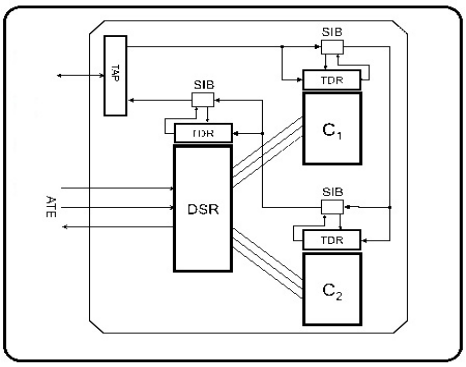

Fig.1. Using IJTAG network to transfer control data.

II. PREVIOUS STUDY

SC test atmosphere with on-nick compression. In line with the control data created with a test scheduler. Because the scan routing pathways in the nick-level test pins towards the core-level test pins are dynamically selected by designs, this interconnection network can also be known to like a dynamic scan router (DSR). The SC test atmosphere of the paper comprises two switching systems, as introduced. An exterior ATE In funnel feeds an In-switching network that reroutes compressed test data to various cores. Identical modules may share exactly the same test data within the broadcast mode. Additionally to individual EDT decompresses, each core features X-masking logic safeguarding its response compactor against unknown states and hooking up the main by having an output-switching network [2]. This network enables the compressed output streams from successive cores to achieve an output funnel, and also to be delivered back towards the ATE. To be able to facilitate test pattern reuse, test wrappers isolate all cores so they are separate from one another. The In DSR includes DE multiplexers whose number matches the amount of ATE In channels. Given several test designs, each DE multiplexer connects the related funnel to one of many destination cores, as shown by the information of address register. The amount of ATE In channels can't be smaller sized compared to capacity from the biggest single core when it comes to its EDT In. Clearly, within the worst situation, we are able to still test the

biggest cores, individually. Typically, low-order by each core are utilized more others. Hence, OR gates are deployed to make sure these In will get data from greater than a single ATE funnel to improve versatility of the test scheduler. Because of the ATE In channels, the connected multiplexers, and all sorts of cores with OR gates driving their EDT In, the particular connections between these terminals are arranged the following. The EDT in are associated with the multiplexers in a way that n EDT By confirmed core are associated with n different ATE In channels, and every ATE funnel serves roughly exactly the same quantity of cores. This process yields the particular size the in multiplexers as well as their control registers [3]. Some final adjustments inside a single module will also be easy to simplify the resultant DSR layout and steer clear of pricey and lengthy connections. The entire process of developing the bottom class terminates when either there aren't any more setup classes complementary using the base, or among the constraints can't be satisfied. It may be further reordered to group tests for the similar core in contiguous time times, finally developing test designs showing which ATE channels will be to interact with which EDT channels which cores as well as for how lengthy. The merging formula removes then your first element from list L and tries to form another base cluster before the listing of setup classes becomes empty, by which situation the scheduling formula returns a summary of base classes that determines the particular schedule.

III. METHODOLOGY

The IEEE 1687 is really a suggested standard for being able to access on-nick make sure debug features through the IEEE 1149.1 test access port. The objective of this internal Joint Test Action Group (IJTAG) standard would be to automate the way in which it's possible to manage on-nick instruments, and also to describe a language for interacting together through the IEEE 1149.1 test data registers (TDRs). Consequently, we start this paper by examining three alternative schemes you can use to upload control bits and show the way they determine the ultimate SC test logic architecture. If there's an IJTAG network on the SC, and also the final amount of test designs is comparatively small, it's possible to utilize it to provide the control data, The SC design uses two devoted control chains to provide the control data. In principle, these structures are acquired by daisy chaining address registers of both DSRs [4]. It's possible to also employ the standard scan channels to provide controls through pipelining stages. For every funnel, this method concatenates n m control bits. The architecture supports as numerous test designs as needed. However, the control information is always submitted with the ATE channels as a fundamental element of an evaluation vector. Hence, given an evaluation configuration, exactly the same control information is repeated for those test designs [5]. The quantity of control information is small, though, as the amount of control bits per funnel is usually a small fraction from the test pattern shift cycles. The schemes suggested within this paper were examined on the large industrial SC design composed of 281 isolated cores.

IV. CONCLUSION

The suggested solutions include techniques accustomed to deliver control data and test scheduling calculations minimizing the general test application time. As proven within this paper, the I/O sources supplied by a tester could be dynamically allotted to selected cores, whereas the entire quantity of channels being used may remain unchanged. This paradigm clearly requires efficient schemes minimizing the general test application time, while considering physical constraints, particularly, SC pin allocations. As Moore's law is constantly on the provide smaller sized products, designs with a variety of core counts, capacity per core, and per core create a dramatic effect on SC design and test methods. Presuming that SC cores are wrapped testable models, this paper studies several practical issues regarding SC-based testing that deploys on-nick test data compression having the ability to dynamically

use ATE channels. Experimental results acquired for any large industrial SC design confirm practicality from the suggested schemes as well as their capability to trade-off the amount of test pins, design complexity from the TAM, and test application time.

REFERENCES

I. S. K. Goel, E. J. Marinissen, A. Sehgal, and K. Chakrabarty, "Testing of SoCs with hierarchical cores: Common fallacies, test access optimization, and test scheduling," *IEEE Trans. Comput.*, vol. 58, no. 3, pp. 409–423, Mar. 2009.

II. E. Larsson and H. Fujiwara, "System-on-chip test scheduling with reconfigurable core wrappers," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 14, no. 3, pp. 305–309, Mar. 2006.

III. J. Janicki, G. Mrugalski, J. Rajski, and J. Tyszer, "Bandwidth-aware test compression logic for SC designs," in *Proc. 17th IEEE Eur. Test Symp. (ETS)*, May 2012, pp. 14–19.

IV. M. Richter and K. Chakrabarty, "Test pin count reduction for NoC-based test delivery in multicore SOCs," in *Proc. Design, Autom. Test Eur. Conf. Exhibit. (DATE)*, 2012, pp. 787–792.

V. Q. Zhou and K. J. Balakrishnan, "Test cost reduction for SC using a combined approach to test data compression and test scheduling," in *Proc. Des., Autom. Test Eur. Conf. Exhibit. (DATE)*, 2007,pp. 39–44.

