A LOW POWER AND HIGH GAIN TWO STAGE FINFET AMPLIFIER

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Abstract— In this paper, a high gain and low-power FINFET-based amplifier with shorted gates is proposed and its design is made in cadence tools with 18nm technology. The main characteristics of the proposed amplifier are such as gain, power consumption, CMRR (common-mode rejection ratio), parametric analysis were calculated and compared with a conventional CMOS two-stage amplifier. It was observed that the proposed FINFET-based amplifier had higher performance at lower supply voltage compared to conventional MOSFET-based two-stage amplifier. In the proposed design with the supply voltage of 1 V for FINFET and 1.7V for CMOS. By comparing the proposed design with conventional CMOS two stage amplifier in terms of figure of merit.

Keywords—CMMR, Parametric, Two stage, Miller capacitor

I. INTRODUCTION

Operational Amplifiers (Op-Amps) is one of the most usage blocks in wide range of analog and mixed-signal systems. They are used in DC bias to high-speed amplifiers and filters. Designing an amplifier with high gain and bandwidth is very hard. According, to the required specifications, several structures of operational amplifier are designed. Basically, operational amplifiers are voltage amplifiers which are used to achieve high gain by applying differential inputs. The gain is usually between 40 to 50 dB. Given that new generations of CMOS technology they tend to have smaller transistor channel length and low supply voltage value, designing operational amplifiers is a challenge for designers. Today, by reducing transistor channel length to a few tens of nanometers, optimization of analog circuits has become difficult. Due to the intrinsic trans-conductance of the CMOS devices as well as gain reduction due to the effects of short channel appeared in sub-micron CMOS processes. Multistage amplifiers may also be used to enhance analog circuits’ gain. However multistage amplifiers usually have a compensation problem. Several compensation designs have been introduced and reported in the literature for multistage amplifiers.

To overcome the problem of MOSFET size reduction in the field of nanoscale, ITRS introduced an alternative to implementation of such structures as fully depleted SOI with ultra-thin body and multi gate MOSFET’s (FINFETs) to the industry. FINFET is a new alternative structure for MOSFET that allows the transistors to be scaled into smaller sizes and has many advantages over MOSFET such as higher drain current, lower switching voltage and 90% reduction in static leakage current. Improved circuit speed and power supply. These effects can overcome double gate mosfets also. The main idea of double-gate MOSFET is that we should have a narrow Si channel and control Si channel by applying the gate contacts to the both sides of the channel. The double-gate concept can be gained by FDSOI structure. If the buried oxide thickness to the gate dielectric is reduced and the ground plate is electrically connected to the transistor's gate, the grounded plate acts as the second gate. The double-gate structure is formed as non-doping channel that is surrounded by the gate electrodes on both sides.
II. FINFET DEVICE

FINFET is defined (classified) as a multi-gate device. The operating mode is much similar to traditional MOSFET. Typically, a source, a drain and a gate are required to control the current. The channel is made between FINFET source and drain which is in form of a three-dimensional strip on top of silicon substrate (the so-called Fin). With the aim of forming multiple gate electrodes on each side that reduces leakage effects and increases the drive current, the gate is covered around the channel as Figure 1. Also, in previous studies researchers have observed that multi gate devices FinFET have a better immunity against variations which might lead to the self-balance of the two gates. FinFET devices are produced in different types. In shorted-gate FinFETs (SG-FinFETs), two gates are connected together and lead to the formation of a three-terminal device. It can be used as a direct alternative for traditional bulk-CMOS devices. In independent-gate FinFETs (IG-FinFETs) the upper part of the gate is delayered and provides two independent gates. Since, the two independent gates can be controlled separately.

2.0 INDEPENDENT GATE:

IG FINFETs as four-terminal (4T) FINFETs. IG FINFETs, the gates are physically isolated. IG FinFETs offer the flexibility of applying different signals or voltages to their two gates. This enables the use of the back-gate bias to modulate the $V_{th}$ of the front gate linearly. However, IG FINFETs incur a high area penalty due to the need for placing two separate gate contacts.

2.1 SHORTED GATE:

In shorted-gate FinFETs (SG-FinFETs), two gates are connected together and lead to the formation of a three-terminal device. It can be used as a direct alternative for traditional bulk-CMOS devices. SG are FinFETs are also known as three-terminal(3T)FinFET. In SG FinFETs, both the front and back gates are physically shorted. Thus, in SG FinFETs, both gates are jointly used to control the electrostatics of the channel. Hence, SG FinFETs show higher on-current ($I_{on}$) and also higher off-current ($I_{off}$ or the subthreshold current) compared to those of IG FinFETs. SG FinFETs can be further categorized based on asymmetries in their device parameters. Normally, the work functions (Φ) of both the front and back gates of a FinFET are the same. However, the work functions can also be made different. This leads to an asymmetric gate-work function SG FINFET or ASG FINFET. ASG FINFETs can be fabricated with selective doping of the two gate stacks. They have very promising short-channel characteristics and have two orders of magnitude lower $I_{off}$ compared to that of an SG FINFET, with $I_{on}$ only somewhat lower than that of an SG FINFET.

![Figure 1](image)

Figure 1. (a) shorted gate (b) independent gate
III. DESIGN AND OUTPUTS

In this paper the comparison of gains, CMRR, PSSR and Power in both CMOS and FINFET. We know that CMOS has effects with short channel circuits whereas the FINFET is overcome all these side effects. However the gain, CMRR of FINFET is greater than the CMOS, the power of FINFET is less than the CMOS.

Figure 2…block diagram

Figure 3 …circuit diagram

1) M1, M2, M3, M4 and M5 form the first stage of amplifier
2) M1 and M2 are differential pair and M3 and M4 are used as the load for the differential pair transistors
3) M6 and M7 together play the role of common source amplifier and form the second stage of amplifier
4) M5 plays the role of current source to the amplifier.
5) M8 together with Ibias plays the role of bias circuit for the amplifier. Cc is used for Miller compensation in the amplifier structure.
CMOS:

![Figure 4: Schematic Diagram](image)

FINFET:

![Figure 5: Schematic Diagram](image)
IV. OUTPUTS

CMOS:

Calculation:
CMRR:

34.17dB
Power Consumption:
Power consumption = average current × supply voltage
= 21.58×10⁻³ W

FINFET:
Figure 10...Differential Gain

Calculation:
CMRR:

69.5dB

Figure 11...Parametric Analysis

Power Consumption:
Power consumption = average current × supply volatage
= 3.349×10⁻³V
INDEPENDENT GATE:

Figure 12...Schematic Diagram

Figure 13...Common Gain
**Figure 14.** Differential Gain

**Calculation:**

**CMRR:**

58.10 dB

**Figure 15.** Parametric Analysis

**Power Consumption:**

Power consumption = average current × supply voltage

= 1.919 × 10⁻⁶ V

**Output values:**
COMPARISON OF CMOS AND FINFET:

<table>
<thead>
<tr>
<th>TRANSiTOR</th>
<th>INPUT VOLATAGES V1,V2 (V)</th>
<th>PROCESS (nm)</th>
<th>GAIN</th>
<th>CMRR (dB)</th>
<th>POWER (mw)</th>
<th>VDD (mw)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMOS</td>
<td>1.7, 1.4</td>
<td>90</td>
<td>103.9</td>
<td>34.17dB</td>
<td>21.58mw</td>
<td>1.8</td>
</tr>
<tr>
<td>FINFET</td>
<td>1.0, 0.8</td>
<td>18</td>
<td>3.9</td>
<td>69.4</td>
<td>15mw</td>
<td>1.8</td>
</tr>
<tr>
<td>INDEPENDENT GATE</td>
<td>1.0, 0.8</td>
<td>18</td>
<td>160</td>
<td>58.10</td>
<td>1.919µw</td>
<td>1.8</td>
</tr>
</tbody>
</table>

V. CONCLUSION

In this paper, FINFET was investigated in the two stage amplifier. Accordingly, the two stage CMOS process was designed in 90nm technology and the proposed amplifier in 18nm FINFET and double-gate transistors with independent gate was designed and simulated by the supply voltage of 1V. Variations in the supply voltage for CMOS are from 1.7 V to 1.4 V and for FINFET is from 1V to 0.8V. In both structures the capacitance load value was 4.4pF and the compensation capacitor value in both designs was 20pF. According to our results, the proposed FINFET amplifier has better results than the two stage CMOS. Independent gate amplifiers are used in less power applications while shorted gate FINFET and CMOS amplifiers are used in high power applications.

REFERENCES


