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A Modified Three-phase Current Source Inverter for Modular Photovoltaic Applications

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Abstract:This paper proposes a circuit topology of a single-stage three-phase current-source photovoltaic (PV) grid-connected inverter with high voltage transmission ratio (VTR). Also, an improved zone sinusoidal pulse width modulation (SPWM) control strategy and an active-clamped sub circuit that can suppress the energy storage switch's turn-off voltage spike are introduced. The circuit topology, control strategy, steady principle characteristics, and high-frequency switching process are analyzed profoundly, as well as the VTR's expression and design criterion of the center-tapped energy storage inductor. The improved zone SPWM control strategy consists of two control loops, namely, the outer loop of input dc voltage of PV cells with the maximum power point tracking and the inner loop of the energy storage inductor current. The experimental results of a 3-kW 96VDC/380V50Hz3φAC prototype have shown that this kind of a three-phase inverter has the excellent performances such as single-stage power conversion, high VTR and power density, and high conversion efficiency. Nonetheless, it has small energy storage inductor and output CLfilter, low output current total harmonic distortion, and flexible voltage con-figuration of the PV cells. This study provides an effective design method for single-stage three-phase inverting with high VTR.

Index Terms—Current source, high voltage transmission ratio (VTR), photovoltaic (PV) grid-connected inverter, three-phase,zone Sinusoidal Pulse width modulation (SPWM) control strategy.

I. INTRODUCTION

The photovoltaic (PV) grid-connected power generation systems commonly adopt the voltage source circuit, which requires the value of dc voltage higher than the peak value of ac voltage. Therefore, an obvious defect arises. When the output capability of the PV cells weakens, i.e., in rainy day or at night, the operation of the whole system stops, along with the decrease of its utilization rate. PV cells operate as current source, therefore, the current-source inverter (CSI) is more suitable for the PV power generation system. Compared with the voltage-source inverter, the CSI has the following characteristics. boosting feature, the input dc current can be manipulated by controlling the magnetizing time of the energy storage inductor, so as to realize the whole process of light utilization from weak to strong. direct control of the output current, thus it is more convenient and reliable to realize maximum power point

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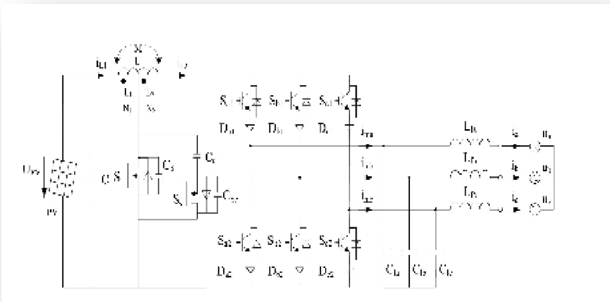
tracking (MPPT), yet the voltage source inverter can cause adc bus crash and the reliability is accordingly reduce. Inductor as the energy storage component, thus the system operation time is longer than that of the voltage source inverter, which uses the electrolytic capacitor as energy storage component. Timely protection for over current, which provides a high reliability.

The single-stage three-phase current-source PWM inverter with low voltage transmission ratio (VTR) proposed in [12]–[17] has the advantages of single-stage power conversion, boosting feature, and timely over current protection, but there still exists the flaws. The VTR is not high enough, and the output waveform quality and conversion efficiency will be seriously affected when the input voltage is too low or the input volt-age variation range is too wide. For example, a 120–200VDC/380V50Hz3φAC inverter can be achieved, but when the input voltage is lower than 120 V, the duty ratio Disclose to the limit value, 1–Dis too small, thus the adjusting range of Dis limited. This would cause some problems such as poor dynamic characteristics, decrease of the VTR caused by the circuit parasitic parameters, large energy storage inductor current and circuit loss, low conversion efficiency, and worse output waveform. Therefore, it is difficult to invert for low voltage of the PV cells. In order to overcome the limitations of the traditional volt-age source PWM inverter [1]–[6] and single-stage three-phase current-source PWM inverter with low VTR [12]–[17], this pa-per proposes a single-stage three-phase CSI with high VTR, as well as the circuit topology and an improved zone sinusoidal pulse width modulation (SPWM) control strategy with two control loops. The loops are consisted of the outer loop of input dc voltage with MPPT and the inner loop of the storage inductor current. Besides, an active-clamped sub circuit that can suppress the energy storage switch's turn-off voltage spike is discussed in this paper, with important conclusions obtained.The photovoltaic (PV) grid-connected power generation systems commonly adopt the voltage source Circuit, which requires the value of dc voltage higher than the peak value of ac voltage. Therefore, an obvious defect arises



Circuit topology of a single-stage three-phase current-source PV grid-connected inverter with high VTR

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II. CIRCUIT TOPOLOGY AND CONTROL STRATEGY

The circuit topology of a single-stage three-phase current-source PV grid-connected inverter with high VTR. The circuit topology is sequentially cascaded by the inputfilter capacitor C, the center-tapped energy storage inductor L, three-phase inverting bridge with six serial blocking diodes and an output CL filter. An energy storage switch Sis connected between the center tap of L and the negative end of the PV cells, the left and right turns number ofLareN1andN2, respectively. Compared to CSI with low VTR [12]–[17], a center tap of the energy storage inductor and an energy storage switch are added to the proposed CSI. An active-clamped sub circuit connected in parallel at both ends of S is proposed, in order to suppress the turn-off voltage spike of S, which is caused by the leakage inductor ofL1. The active-clamped sub circuit is consisted of active-clamped switch Scand a serial clamping capacitor Cc. The VTR of the proposed CSI depends on both the energy storage duty ratio and the center tap position of L, and it provides a possibility to realize high VTR inverting.

III STEADY PRINCIPLE

There are six operating intervals in a line cycle of the inverter,and each interval can be divided into three operating modes.

Taking the Interval I in the Table I as an example, three operatingmodes of the inverter. WhenSb2is ON,Sa2,Sc2, andSb1are OFF.Mode I-1:S is ON,Sa1andSc1are OFF. Energy is stored toL1andiL1increases linearly with the rate ofUPV/L1via thepath ofUPV,L1, andS.ia,ib, andicare maintained byCfa,Cfb, andCfc.Mode I-2:Sa1is ON,SandSc1are OFF. Sinceuab>UPV,Ildecreases linearly at the rate of(uab−UPV)/Lvia the pathofUPV,L, andSa1.UPVandLdeliver energy to the gridsimultaneously.icis maintained byCfc.Mode I-3:Sc1is ON, S andSa1are OFF. Sinceucb>UPV,iLdecreases linearly with the rate of(ucb−UPV)/Lvia thepath ofUPV,L, andSc1,UPVandLdeliver energy to the gridsimultaneously.iais maintained byCfa.In a line cycle, the sequence of operating intervals for theinverter is I–VI, where the sequence of operating modes inInterval I is I–1, I–2, I–1, and I–3. Sequence of operating modesin other intervals is similar.. An energy storage switch Sis connected between the center tap of L and the negative end of the PV cells, the left and right turns number ofLareN1andN2, respectively. Compared to CSI with low VTR [12]–[17], a center tap of the energy storage inductor and an energy storage switch are added to the proposed CSI.

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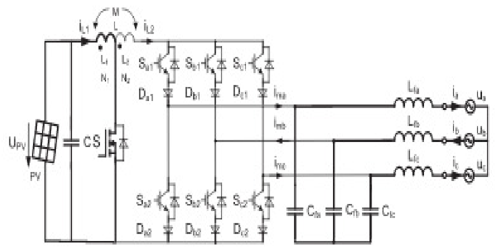
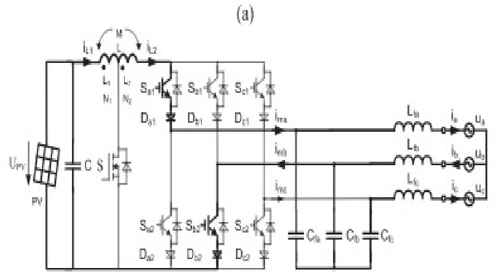


(a)



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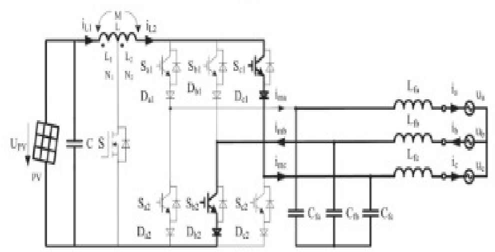
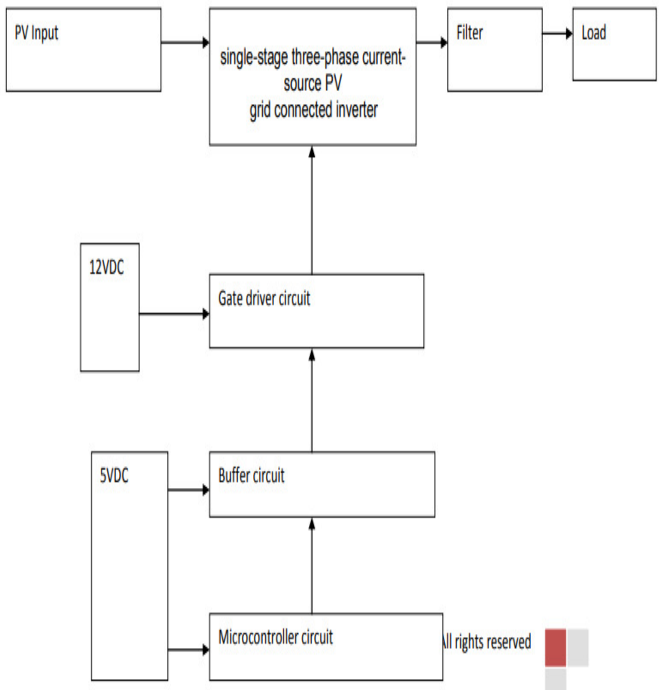


(c)

IV BLOCK DIAGRAM EXPLANATION

A single-stage three-phase CSI with high VTR is Proposed as well as the circuit topology and an improved zone sinusoidal pulse width modulation (SPWM) control strategy with two control Loops. The loops are consisted of the outer loop of input dc voltage with MPPT and the inner loop of the storage inductor current. The circuit topology of a single-stage three-phase current source PV grid-connected inverter with high VTR . The active-clamped subcircuit is consisted of active-clamped switch Sc and a serial clamping capacitor Cc . The VTR of the proposed CSI depends on both the energy storage duty ratio and the center tap position of L, and it provides a possibility to realize high VTR inverting.



V GATE DRIVER CIRCUIT

A gate driver is a power amplifier that accepts a low-power input from a controller IC and produces a high-current drive input for the gate of a high-power transistor such as an IGBT or power MOSFET. Gate drivers can be provided either on-chip or as a discrete module. In essence, a gate driver consists of a level shifter in combination with an amplifier.When a transistor is switched on or

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off, it does not immediately switch from a non-conducting to a conducting state; and may transiently support both a high voltage and conduct a high current. Consequently, when gate current is applied to a transistor to cause it to switch, a certain amount of heat is generated which can, in some cases, be enough to destroy the transistor. Therefore, it is necessary to keep the switching time as short as possible, so as to minimize switching loss. Typical switching times are in the range of microseconds. The switching time of a transistor is inversely proportional to the amount of current used to charge the gate. Therefore, switching currents are often required in the range of several hundred milli amperes, or even in the range of amperes. For typical gate voltages of approximately 10-15V, several watts of power may be required to drive the switch. When large currents are switched at high frequencies, e.g. in DC-to-DC converters or large electric motors, multiple transistors are sometimes provided in parallel, so as to provide sufficiently high switching currents and switching power. The switching signal for a transistor is usually generated by a logic circuit or a microcontroller, which provides an output signal that typically is limited to a few milliamperes of current. Consequently, a transistor which is directly driven by such a signal would switch very slowly, with correspondingly high power loss. During switching, the gate capacitor of the transistor may draw current so quickly that it causes a current overdraw in the logic circuit or microcontroller, causing overheating which leads to permanent damage or even complete destruction of the chip. To prevent this from happening, a gate driver is provided between the microcontroller output signal and the power transistor.

VI BUFFER CIRCUIT

A buffer amplifier (sometimes simply called a buffer) is one that provides electrical impedance transformation from one circuit to another, with the aim of preventing the signal source from being affected by whatever currents (or voltages, for a current buffer) that the load may produce. The signal is 'buffered from' load currents. Two main types of buffer exist: the voltage buffer and the current buffer.

VII MICROCONTROLLER CIRCUIT

A microcontroller (MCU for *microcontroller unit*, or UC for *μ-controller*) is a small computer on a single integrated circuit. In modern terminology, it is similar to, but less sophisticated than, a system on a chip (SoC); anSoC may include a microcontroller as one of its components. A microcontroller contains one or more CPUs (processor cores along with memory and programmable input/output peripherals. Program memory in the form of ferroelectric RAM, NOR flash or OTP ROM is also often included on chip, as well as a small amount of RAM.

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Microcontrollers are designed for embedded applications, in contrast to the microprocessors used in personal computers or other general purpose applications consisting of various discrete chips.

VIII CONCLUSION

The circuit topology of the proposed inverter is a sequentially cascaded of the input filter capacitor, the center-tapped energy storage inductor, three-phase inverting bridge with six serial blocking diodes, and output CL filter, with an energy storage switch connected between the center tap of L and the negative end of the input source. The proposed two-loop improved zone SPWM control strategy can ensure the normal operation of the CSI in any HF switching period with the condition that output line voltage are not smaller than input voltage, i.e.,√6/2Up≥UPV, and the reactive power adjustment of the system is realized.There are six operating intervals in one output line frequency period, eachoperating interval has three operatingmodes; the VTR expression is derived, which can be adjusted through the coefficientK=kILavgand the turnsratioN2/N1ofL. The active clamped sub circuit can effectively suppress the turn-off voltage spike of S caused by the leakage inductor, and there are 14 different operating intervals within one HF switching periodTs. The design criterion of the center-tapped energy storage inductor is derived.6) The designed 3-kW 96VDC/380V50Hz3φAC PV grid-connected inverter prototype has excellent performance s such as higher VTR, much smaller energy storage inductor and higher conversion efficiency, and the experimental results validate theoretical analysis.

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