

A Cost Effective PFC Bridgeless Buck–Boost Converter-Fed BLDC Motor Drive

B Vijay Kumar Reddy¹, CH.Mahesh Reddy²,

¹Assistant Professor Dept. of EEE, Nalla Narasimha Reddy Group of Institutions, Hyderabad, T.S, India, vijaykumarreddy

²Assistant Professor Dept. of EEE, Nalla Narasimha Reddy Group of Institutions, Hyderabad, T.S, India,

Abstract—This paper presents a cost-effective solution for low-power applications using power factor corrected (PFC) bridgeless (BL) buck–boost converter-fed brushless direct current (BLDC) motor drive. An attempt of speed control of the BLDC motor is done by controlling the dc link voltage of the voltage source inverter (VSI). With the help of a single voltage sensor, the operation of VSI at fundamental frequency switching by using the electronic commutation of the BLDC motor which offers reduced switching losses. A BL configuration of the buck–boost converter offers the elimination of the diode bridge rectifier, thus reducing the conduction losses associated with it. The system is designed to operate in discontinuous inductor current mode (DICM) to provide an inherent PFC at ac mains. The performance of the drive is evaluated over a wide range of speed control and varying supply voltages (universal ac mains at 90–265 V) with improved power quality at ac mains. The obtained power quality indices are within the acceptable limits of international power quality standards such as the IEC 61000 -3-2. The performance of the proposed drive is simulated in MATLAB/Simulink environment, and the obtained results are validated experimentally on a developed prototype of the drive.

Index Terms—Bridgeless (BL) buck–boost converter, brushless direct current (BLDC) motor, discontinuous inductor current mode (DICM), power factor corrected (PFC), power quality.

I. INTRODUCTION

Cost and efficiency are the major concerns in the improving and manufacturing of low-power motor drives targeting household applications such as fans, water pumps, blowers, mixers, etc. The use of the BLDC motor in these applications is becoming very common due to features of low maintenance requirements, high flux density per unit volume, high efficiency, and low electromagnetic-interference problems. Not only to household applications, but also these BLDC motors are suitable for other applications such as transportation, HVAC, medical equipment, motion control and many industrial tools.

The BLDC motor is also known as an electronically commutated motor because an electronic commutation based on rotor position is used rather than a mechanical commutation which has disadvantages like sparking and wear and tear of brushes and commutator assembly. BLDC motor has three phase windings on the stator and permanent magnets on the rotor.

The conventional PFC scheme of the BLDC motor drive utilizes a pulsewidth-modulated voltage source inverter (PWM-VSI) for speed control with a constant dc link voltage. This offers higher switching losses in VSI as the switching losses increase as a square function of switching frequency. As the speed of the BLDC motor is directly proportional to the applied dc link voltage, hence, the speed

control is achieved by the variable dc link voltage of VSI. This allows the fundamental frequency switching of VSI (i.e., electronic commutation) and offers reduced switching losses.

The choice of mode of operation of a PFC converter is a critical issue because it directly affects the cost and rating of the components used in the PFC converter. The continuous conduction mode (CCM) and discontinuous conduction mode (DCM) are the two modes of operation in which a PFC converter is designed to operate. In CCM, the current in the inductor or the voltage across the intermediate capacitor remains continuous, but it requires the sensing of two voltages (dc link voltage and supply voltage) and input side current for PFC operation, which is not cost-effective. On the other hand, DCM requires a single voltage sensor for dc link voltage control, and inherent PFC is achieved at the ac mains, but at the cost of higher stresses on the PFC converter switch; hence, DCM is preferred for low-power applications.

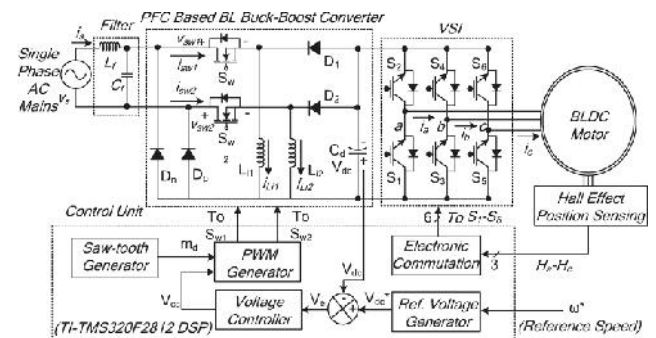


Fig. 1. BLDC motor drive with front-end BL buck–boost converter

II. PFC BL BUCK–BOOST CONVERTER-FED BLDC MOTOR DRIVE

Fig. 1 shows the proposed BL buck–boost converter-based VSI-fed BLDC motor drive. The parameters of the BL buck–boost converter are designed such that it operates in discontinuous inductor current mode (DICM) to achieve an inherent power factor correction at ac mains. The speed control of BLDC motor is achieved by the dc link voltage control of VSI using a BL buck–boost converter. This reduces the switching losses in VSI due to the low frequency operation of VSI for the electronic commutation of the BLDC motor. The performance of the proposed drive is evaluated for a wide range of speed control with improved power quality at ac mains. Moreover,

the effect of supply voltage variation at universal ac mains is also studied to demonstrate the performance of the drive in practical supply conditions. Voltage and current stresses on the PFC converter switch are also evaluated for determining the switch rating and heat sink design. Finally, a hardware implementation of the proposed BLDC motor drive is carried out to demonstrate the feasibility of the proposed drive over a wide range of speed control with improved power quality at ac mains.

TABLE I
COMPARATIVE ANALYSIS OF PROPOSED BL BUCK-BOOST CONVERTER WITH EXISTING TOPOLOGIES

Configuration	No. of Devices					$\frac{1}{2}$ Period Cond.	Suitability
	S_w	D	L	C	Total		
BL-Buck [13]	2	4	2	2	10	5	No
BL-Boost [14]	2	2	1	1	6	4	No
BL-Boost [15]	2	2	1	2	7	7	No
BL-Buck-Boost [16]	3	4	1	3	11	8	Yes
BL-Cuk T-1 [17, 18]	2	3	3	3	11	7	Yes
BL-Cuk T-2 [17, 18]	2	2	3	4	11	11	Yes
BL-Cuk T-3 [17, 18]	2	4	4	3	13	7	Yes
BL-Cuk [19]	2	3	3	2	10	8	Yes
BL-SEPIC [20]	2	3	1*	3	9	7	Yes
BL-SEPIC [21]	2	3	2	2	9	7	Yes
Proposed	2	4	2	1	9	5	Yes

*- Coupled Inductor

A brief comparison of various configurations reported in the literature is tabulated in Table I. The comparison is carried out on the basis of the total number of components (switch— S_w , diode—D, inductor—L, and capacitor—C) and total number of components conducting during each half cycle of supply voltage. The BL buck and boost converter configurations are not suitable for the required application due to the requirement of high voltage conversion ratio.

The proposed configuration of the BL buck-boost converter has the minimum number of components and least number of conduction devices during each half cycle of supply voltage which governs the choice of the BL buck-boost converter for this application.

III. OPERATING PRINCIPLE OF PFC BL BUCK-BOOST CONVERTER

The operation of the PFC BL buck-boost converter is classified into two parts which include the operation during the positive and negative half cycles of supply voltage and during the complete switching cycle.

A. Operation During Positive and Negative Half Cycles of Supply Voltage

In the proposed scheme of the BL buck-boost converter, switches S_{w1} and S_{w2} operate for the positive and negative half cycles of the supply voltage, respectively. During the positive half cycle of the supply voltage, switch S_{w1} , inductor L_{i1} , and diodes D_1 and D_p are operated to transfer energy to dc link capacitor C_d as shown in Fig. 2(a)–(c). Similarly, for the negative half cycle of the supply voltage, switch S_{w2} , inductor L_{i2} , and diodes

D_2 and D_n conduct as shown in Fig. 3(a)–(c). In the DICM operation of the BL buck-boost converter, the current in inductor L_i becomes discontinuous for a certain duration in a switching period. Fig. 2(d) shows the waveforms of different parameters during the positive and negative half cycles of supply voltage.

B. Operation During Positive and Negative Half Cycles of Supply Voltage

In the proposed scheme of the BL buck-boost converter, switches S_{w1} and S_{w2} operate for the positive and negative half cycles of the supply voltage, respectively. During the positive half cycle of the supply voltage, switch S_{w1} , inductor L_{i1} , and diodes D_1 and D_p are operated to transfer energy to dc link capacitor C_d as shown in Fig. 2(a)–(c). Similarly, for the negative half cycle of the supply voltage, switch S_{w2} , inductor L_{i2} , and diodes D_2 and D_n conduct as shown in Fig. 3(a)–(c). In the DICM operation of the BL buck-boost converter, the current in inductor L_i becomes discontinuous for a certain duration in a switching period. Fig. 2(d) shows the waveforms of different parameters during the positive and negative half cycles of supply voltage.

C. Operation During Complete Switching Cycle

Three modes of operation during a complete switching cycle are discussed for the positive half cycle of supply voltage as shown hereinafter.

Mode I: In this mode, switch S_{w1} conducts to charge the inductor L_{i1} ; hence, an inductor current $i_{L_{i1}}$ increases in this mode as shown in Fig. 2(a). Diode D_p completes the input side circuitry, whereas the dc link capacitor C_d is discharged by the VSI-fed BLDC motor as shown in Fig. 3(d).

Mode II: As shown in Fig. 2(b), in this mode of operation, switch S_{w1} is turned off, and the stored energy in inductor L_{i1} is transferred to dc link capacitor C_d until the inductor is completely discharged. The current in inductor L_{i1} reduces and reaches zero as shown in Fig. 3(d).

Mode III: In this mode, inductor L_{i1} enters discontinuous conduction, i.e., no energy is left in the inductor; hence, current $i_{L_{i1}}$ becomes zero for the rest of the switching period. As shown in Fig. 2(c), none of the switch or diode is conducting in this mode, and dc link capacitor C_d supplies energy to the load; hence, voltage V_{dc} across dc link capacitor C_d starts decreasing. The operation is repeated when switch S_{w1} is turned on again after a complete switching cycle.

Similarly, for the negative half cycle of the supply voltage, switch S_{w2} , inductor L_{i2} , and diodes D_n and D_2 operate for voltage control and PFC operation.

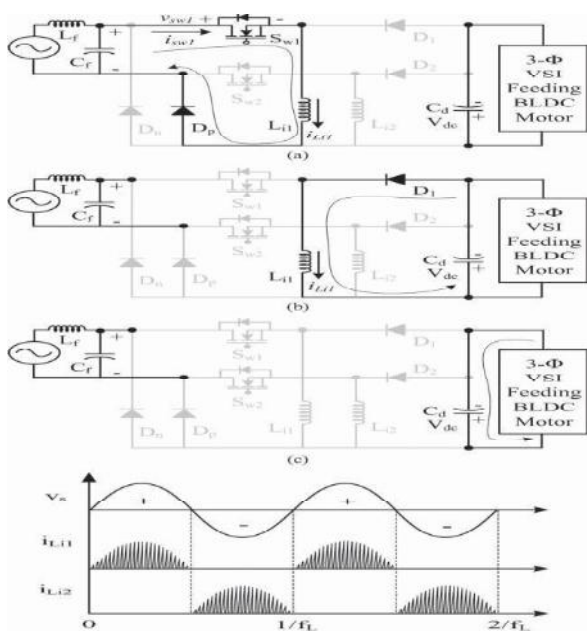


Fig. 2. Operation of the proposed converter in different modes (a)–(c) for a positive half cycle of supply voltage and (d) the associated waveforms. (a) Mode I. (b) Mode II. (c) Mode III. (d) Waveforms for positive and negative half cycles of supply voltage.

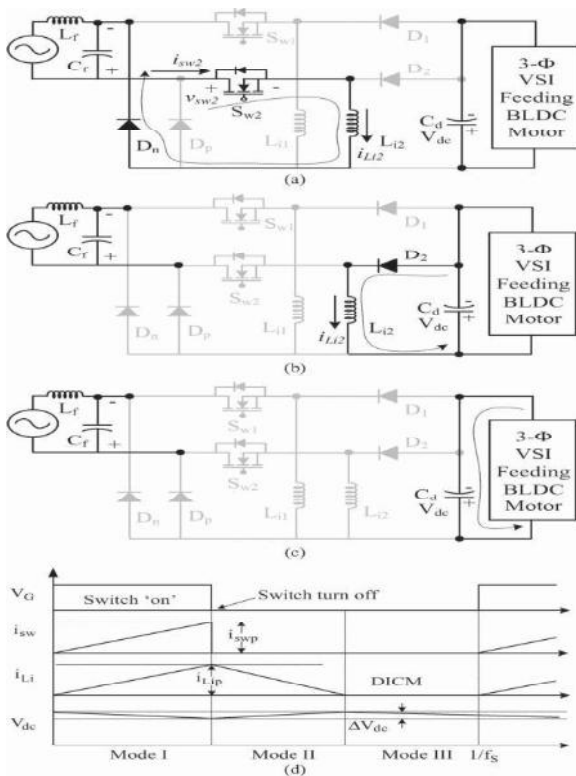


Fig. 3. Operation of the proposed converter in different modes (a)–(c) for a negative half cycle of supply voltage and (d) the associated waveforms. (a) Mode I. (b) Mode II. (c) Mode III. (d) Waveforms during complete switching cycle

IV. CONTROL OF PFC BL BUCK–BOOST CONVERTER-FED BLDC MOTOR DRIVE

The control of the PFC BL buck–boost converter- fed BLDC

motor drive is classified into two parts as follows.

A. Control of Front-End PFC Converter: Voltage Follower Approach

The control of the front-end PFC converter generates the PWM pulses for the PFC converter switches (\$S_{w1}\$ and \$S_{w2}\$) for dc link voltage control with PFC operation at ac mains. A single voltage control loop (voltage follower approach) is utilized for the PFC BL buck–boost converter operating in DICM. A reference dc link voltage (\$V_{dc}^*\$) is generated as

$$V_{dc}^* = k_v \omega^*$$

where \$k_v\$ and \$\omega^*\$ are the motor’s voltage constant and the reference speed, respectively.

The voltage error signal (\$V_e\$) is generated by comparing the reference dc link voltage (\$V_{dc}^*\$) with the sensed dc link voltage (\$V_{dc}\$) as

$$V_e(k) = V_{dc}(k) - V_{dc}^*(k)$$

where \$k\$ represents the \$k\$th sampling instant.

This error voltage signal (\$V_e\$) is given to the voltage proportional–integral (PI) controller to generate a controlled output voltage (\$V_{cc}\$) as

$$V_{cc}(k) = V_{cc}(k - 1) + k_p \{ V_e(k) - V_e(k - 1) \} + k_i V_e(k)$$

where \$k_p\$ and \$k_i\$ are the proportional and integral gains of the voltage PI controller.

Finally, the output of the voltage controller is compared with a high frequency sawtooth signal (\$m_d\$) to generate the PWM pulses as

$$\begin{aligned} \text{For } v_s > 0: & \quad \text{if } m_d < V_{cc} \text{ then } S_{w1} = \text{'ON'} \\ & \quad \text{if } m_d \geq V_{cc} \text{ then } S_{w1} = \text{'OFF'} \\ \text{For } v_s < 0: & \quad \text{if } m_d < V_{cc} \text{ then } S_{w2} = \text{'ON'} \\ & \quad \text{if } m_d \geq V_{cc} \text{ then } S_{w2} = \text{'OFF'} \end{aligned}$$

where \$S_{w1}\$ and \$S_{w2}\$ represent the switching signals to the switches of the PFC converter.

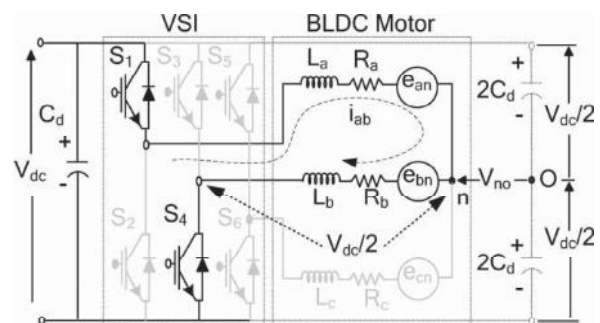


Fig. 4. Operation of a VSI-fed BLDC motor when switches \$S_1\$ and \$S_4\$ are conducting

TABLE II
SWITCHING STATES FOR ACHIEVING ELECTRONIC COMMUTATION OF
BLDC MOTOR BASED ON HALL-EFFECT POSITION SIGNALS

θ ($^\circ$)	Hall Signals			Switching States					
	H _a	H _b	H _c	S ₁	S ₂	S ₃	S ₄	S ₅	S ₆
NA	0	0	0	0	0	0	0	0	0
0-60	0	0	1	1	0	0	0	0	1
60-120	0	1	0	0	1	1	0	0	0
120-180	0	1	1	0	0	1	0	0	1
180-240	1	0	0	0	0	0	1	1	0
240-300	1	0	1	1	0	0	1	0	0
300-360	1	1	0	0	1	0	0	1	0
NA	1	1	1	0	0	0	0	0	0

B. Control of BLDC Motor: Electronic Commutation

An electronic commutation of the BLDC motor includes the proper switching of VSI in such a way that a symmetrical dc current is drawn from the dc link capacitor for 120° and placed symmetrically at the center of each phase. A Hall-effect position sensor is used to sense the rotor position on a span of 60°, which is required for the electronic commutation of the BLDC motor. The conduction states of two switches (S1 and S4) are shown in Fig. 5. A line current i_{ab} is drawn from the dc link capacitor whose magnitude depends on the applied dc link voltage (Vdc), back electromotive forces (EMFs) (e_{an} and e_{bn}), resistances (R_a and R_b), and self-inductance and mutual inductance (L_a, L_b, and M) of the stator windings. Table II shows the different switching states of the VSI feeding a BLDC motor based on the Hall-effect position signals (H_a–H_c).

V. SIMULATED PERFORMANCE OF PROPOSED BLDC MOTOR DRIVE

The performance of the proposed BLDC motor drive is simulated in MATLAB/Simulink environment using the Sim- Power-System toolbox. The performance evaluation of the proposed drive is categorized in terms of the performance of the BLDC motor and BL buck–boost converter and the achieved power quality indices obtained at ac mains. The parameters associated with the BLDC motor such as speed (N), electro- magnetic torque (T_e), and stator current (i_a) are analyzed for the proper functioning of the BLDC motor. Parameters such as supply voltage (V_s), supply current (i_s), dc link voltage (V_{dc}), inductor’s currents (i_{Li1}, i_{Li2}), switch voltages (V_{sw1}, V_{sw2}), and switch currents (i_{sw1}, i_{sw2}) of the PFC BL buck–boost converter are evaluated to demonstrate its proper functioning.

A. Steady-State Performance

The steady-state behavior of the proposed BLDC motor drive for two cycles of supply voltage at rated condition (rated dc link voltage of 200 V) is shown in Fig. 6. The discontinuous inductor currents (i_{Li1} and i_{Li2}) are obtained, confirming the DICM operation of the BL buck–boost converter. The performance of the proposed BLDC motor drive at speed control by varying dc link voltage from 50 to 200 V is tabulated in Table III. The harmonic

spectra of the supply current at rated and light load conditions, i.e., dc link voltages of 200 and 50 V.

B. Dynamic Performance of Proposed BLDC Motor Drive

The dynamic behavior of the proposed drive system during a starting at 50 V, step change in dc link voltage from 100 to 150 V, and supply voltage change from 270 to 170V is shown in Fig. 8. A smooth transition of speed and dc link voltage is achieved with a small overshoot in supply current under the acceptable limit of the maximum allowable stator winding current of the BLDC motor.

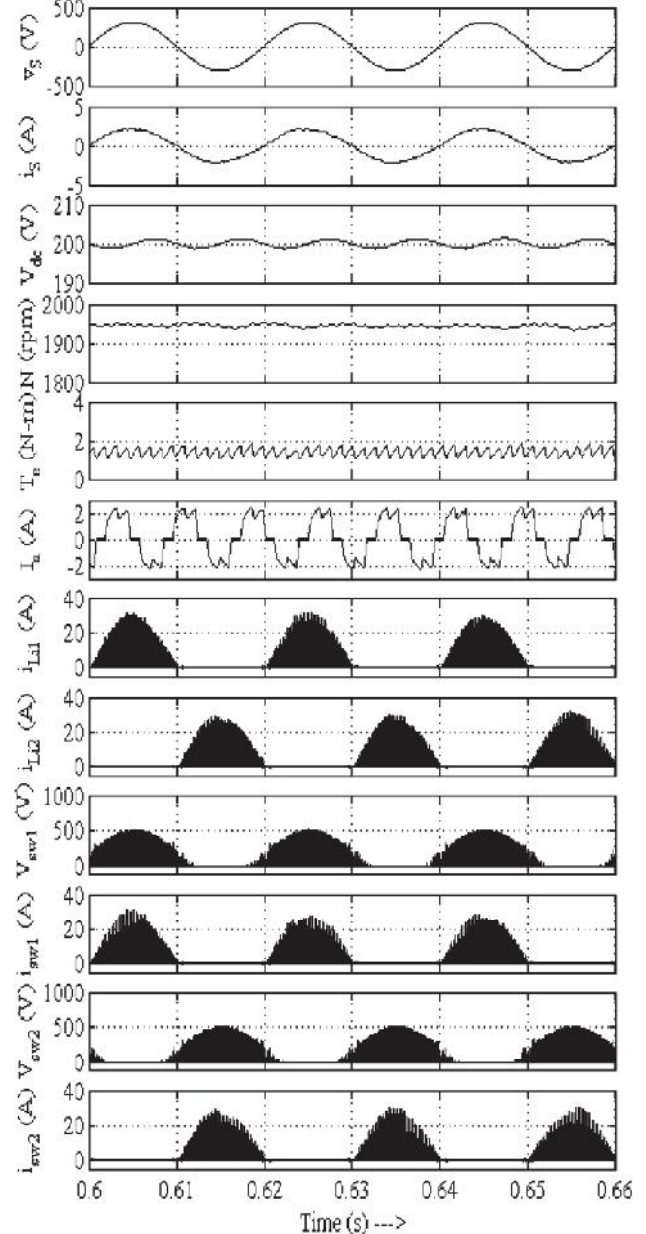


Fig. 5. Steady-state performance of the proposed BLDC motor drive at rated conditions.

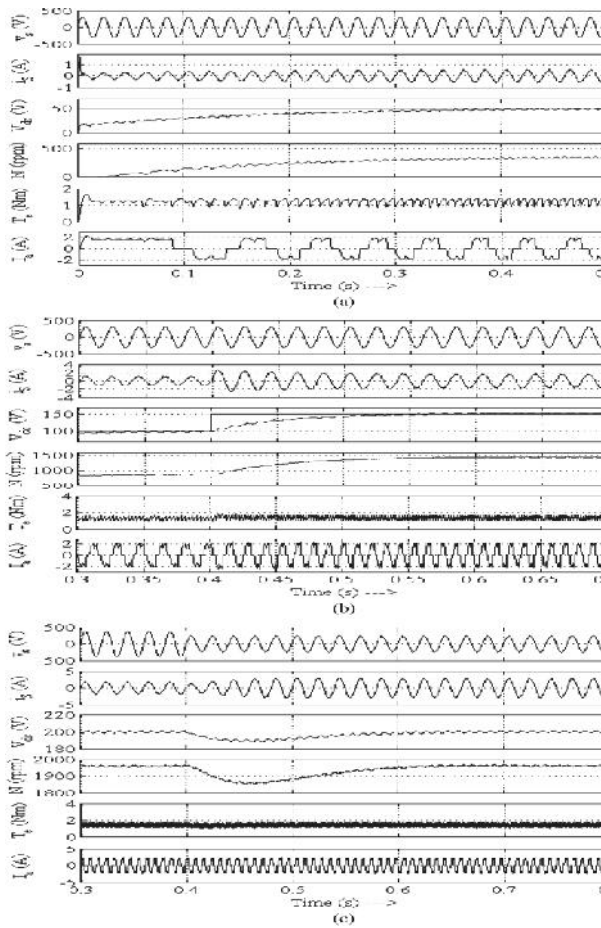


Fig. 6. Dynamic performance of proposed BLDC motor drive during (a) starting, (b) speed control, and (c) supply voltage variation at rated conditions

Block diagram of Extended system

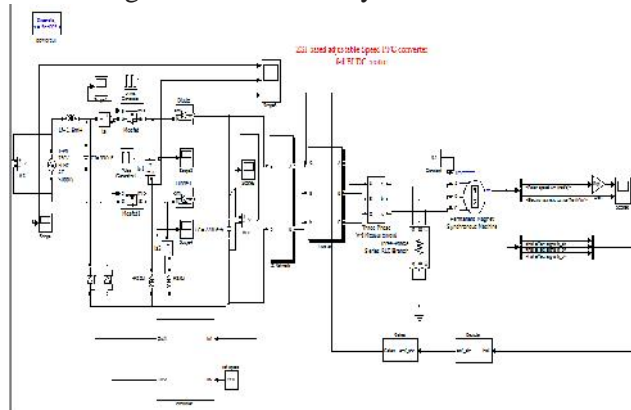


Fig.7 ZSI based adjustable Speed PFC converter fed BLDC motor

Experimental results:

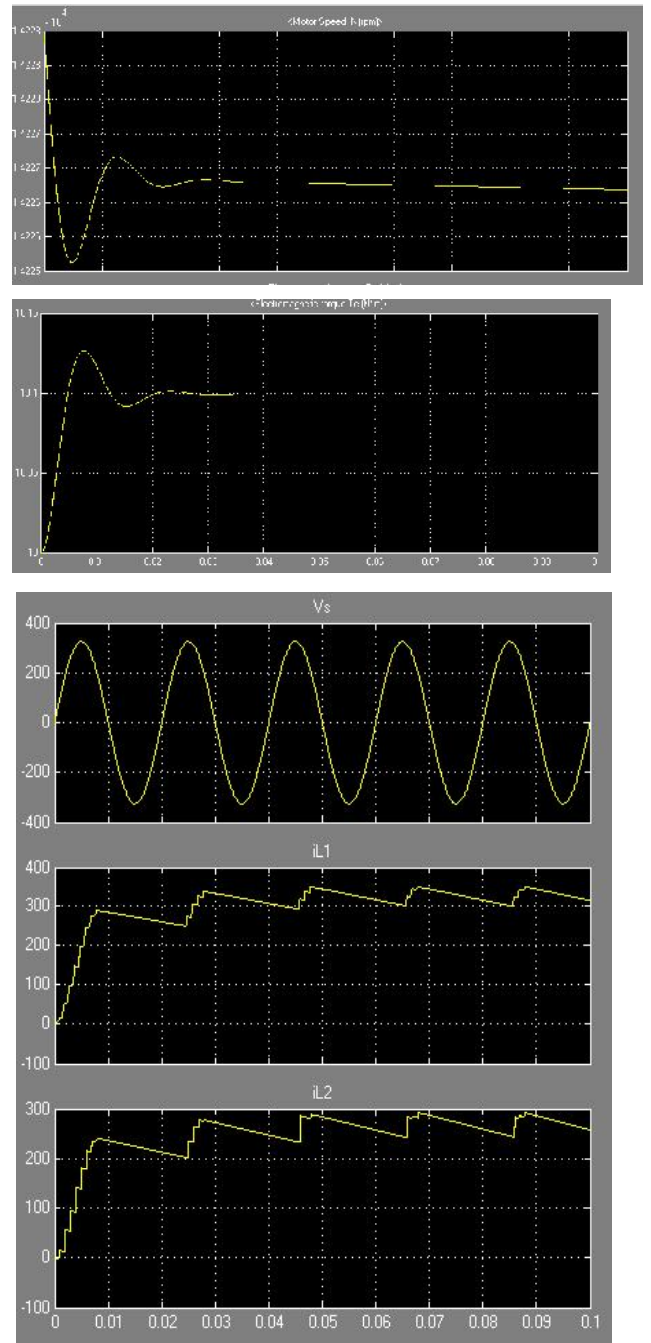


Fig 8.Experimental results of ZSI based adjustable Speed PFC converter fed BLDC motor

VI. CONCLUSION

A PFC BL buck–boost converter-based VSI-fed BLDC motor drive has been proposed targeting low-power applications. A new method of speed control has been utilized by controlling the voltage at dc bus and operating the VSI at fundamental frequency for the electronic commutation of the BLDC motor for reducing the switching losses in VSI. The front-end BL buck–boost converter has been operated in DICM for achieving an inherent power factor correction at ac mains. A satisfactory performance has been achieved for speed control and supply voltage variation with power quality indices within the acceptable limits of IEC 61000-3-2. Moreover, voltage and current stresses on the PFC switch have been evaluated for determining the practical application of the proposed scheme. Finally, an experimental prototype of the proposed drive has been developed to validate the performance of the proposed BLDC motor drive under speed control with improved power quality at ac mains. The proposed scheme has shown satisfactory performance, and it is a recommended solution applicable to low-power BLDC motor drives.

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