

Harmonic reduction in distribution grid by using cascaded based nine-level inverters in PV integrated network

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Abstract : This work proposes a Secondary distribution (single phase) nine -level inverter for grid connected photovoltaic systems, with a novel pulse width modulated (PWM) control scheme. Four reference signals that are identical to each other with an offset that is equivalent to the amplitude of the triangular carrier signal were used to generate the pwm signals the inverter is capable producing nine levels of output-voltage levels (V_{dc} , $3V_{dc}/4$, $V_{dc}/2$, $V_{dc}/4$, 0 , $-V_{dc}$, $-3V_{dc}/4$, $-V_{dc}/2$, $-V_{dc}/4$) from the dc supply voltage. A digital proportional-integral current-control algorithm was implemented in a TMS320F2812 DSP to keep the current injected into the grid sinusoidal. The proposed system was verified through simulation and implemented in a prototype.

Keywords - Grid connected, modulation index, multilevel inverter, photovoltaic (PV) system, pulse width modulated (PWM), total harmonic distortion (THD).

I. INTRODUCTION

The ever-increasing energy consumption, fossil fuels' soaring costs and exhaustible nature, and worsening global environment have created a booming interest in renewable energy generation systems, one of which is photovoltaic. Such a system generates electricity by converting the Sun's energy directly into electricity. Photovoltaic-generated energy can be delivered to power system networks through grid-connected inverters. A single-phase grid-connected inverter is usually used for residential or low-power applications of power ranges that are less than 10 kW. Types of single-phase grid-connected inverters have been investigated. A common topology of this inverter is full-bridge three-level. The three-level inverter can satisfy specifications through its very high switching, but it could also unfortunately increase switching losses, acoustic noise, and level of interference to other equipment. Improving its output waveform reduces its harmonic content and, hence, also the size of the filter used and the level of electromagnetic interference (EMI) generated by the inverter's switching operation. Multilevel

inverters are promising; they have nearly sinusoidal output-voltage waveforms, output current with better harmonic profile, less stressing of electronic components owing to decreased voltages, switching losses that are lower than those of conventional two-level inverters, a smaller filter size, and lower EMI, all of which make them cheaper, lighter, and more compact. Various topologies for multilevel inverters have been proposed over the years. Common ones are diode-clamped, flying capacitor or multi cell, cascaded H-bridge, and modified H-bridge multilevel. This paper recounts the development of a novel modified H-bridge single-phase multilevel inverter that has two diode embedded bidirectional switches and a novel pulse width modulated (PWM) technique. The topology was applied to a grid-connected photovoltaic system with considerations for a maximum-power-point tracker (MPPT) and a current-control algorithm.

II. PROPOSED MULTILEVEL INVERTER

The proposed single-phase nine-level inverter was developed from the seven-level inverter in. It comprises a single-phase conventional H-bridge inverter, two bidirectional switches, and a capacitor voltage divider formed by C_1 , C_2 , C_3 , and C_4 as shown in Fig. 1. The modified H-bridge topology is significantly advantageous over other topologies, i.e., less power switch, power diodes, and less capacitors for inverters of the same number of levels. Photovoltaic (PV) arrays were connected to the inverter via a dc-dc boost converter. The power generated by the inverter is to be delivered to the power network, so the utility grid, rather than a load, was used. The dc-dc boost converter was required. The because the PV arrays had a voltage that was lower than the grid voltage. High dc bus voltages are necessary to ensure that power flows from the PV arrays to the grid. A filtering inductance L_f was used to filter the current injected into the grid. Proper switching of the inverter can produce seven output-voltage levels (V_{dc} , $3V_{dc}/4$, $V_{dc}/2$, $V_{dc}/4$, 0 , $-V_{dc}$, $-3V_{dc}/4$, $-V_{dc}/2$, $-V_{dc}/4$) from the dc supply voltage.

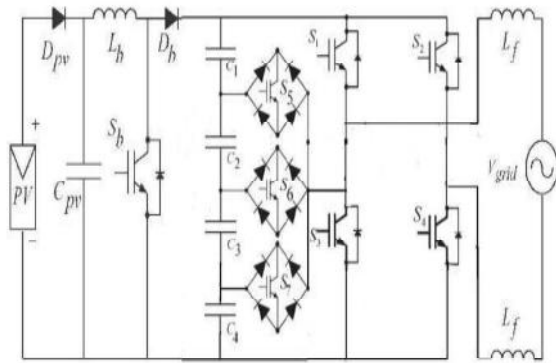


Fig. 1. Proposed single phase nine-level grid-connected inverter for photovoltaic systems.

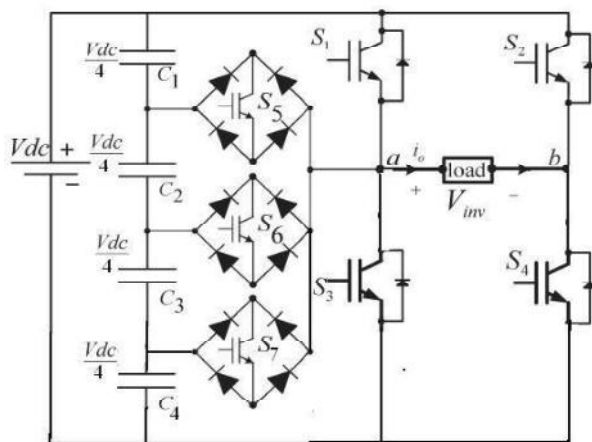


Fig. 2. Nine-level inverter for switching operation.

The single-phase nine-level inverter was developed from the seven-level inverter as shown in Fig.1. It comprises a single-phase conventional H-bridge inverter, three bidirectional switches, and a capacitor voltage divider formed by C1, C2,C3 and

C4, as shown in Fig. 1. The modified H-bridge topology is significantly have advantages converter. The power generated by the inverter is to be delivered to induction Motor. The dc–dc boost converter was required because the PV arrays had a voltage that was lower than the single-phase voltage. High dc bus voltages are necessary to ensure that power flows from the PV arrays to the single-phase induction motor. The LC-filter is modeled to obtain pure sine-wave and is given to drive a single-phase induction motor.. Proper switching of the inverter can produce nine- output-voltage-levels (V_{dc} , $3 V_{dc} / 4$, $V_{dc} / 2$, $V_{dc} / 4$, 0 , $-V_{dc} / 4$, $-V_{dc} / 2$, $-3V_{dc} / 4$, $-V_{dc}$) from the dc supply voltage. The proposed inverter’s operation can be divided into nine switching states. The required nine levels of output voltage were generated as follows.

Maximum positive output (V_{dc}): S1 is ON; connecting the load positive terminal to V_{dc} , and S4 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is V_{dc} .

Three-fourth positive output ($3V_{dc}/4$): The bidirectional switch S5 is ON, connecting the load positive terminal, and S4 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is $3V_{dc}/4$.

Half of the positive output ($V_{dc}/2$): The bidirectional switch S6 is ON, connecting the load positive terminal, and S4 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is $V_{dc}/2$.

One-fourth of the positive output ($V_{dc}/4$): The bidirectional switch S7 is ON, connecting the load positive terminal, and S4 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is $V_{dc}/4$.

Zero output: This level can be produced by two switching combinations; switches S3 and S4 are ON, or S1 and S2 are ON, and all other controlled switches are OFF; terminal ab is a short circuit, and the voltage applied to the load terminals is zero.

TABLE 1 Out Put Voltage

According To The Switches On Off

III CLOSED LOOP CONTROL SYSTEM

The control system comprises a MPPT algorithm, a dc-bus voltage controller, reference-current generation and a current controller. The two main tasks of the control system are maximization of the energy transferred from the PV arrays to the grid, and generation of a sinusoidal current with minimum harmonic distortion, also under the

presence of grid voltage harmonics. The proposed inverter utilizes the perturb-and-observe (P&O) algorithm for its wide usage in MPPT owing to its simple structure and requirement of only a few measured parameters. It periodically perturbs (i.e., increment or decrement) the array terminal voltage and compares the PV output power with that of the

previous perturbation cycle. If the power was increasing, the perturbation would continue in the same direction in the next cycle; otherwise, the direction would be reversed. This means that the array terminal voltage is perturbed every MPPT cycle; therefore, when the MPP is reached, the P&O algorithm will oscillate around it. The P&O algorithm was implemented in the dc–dc boost converter. The output of the MPPT is the duty-cycle function. Fig.3. shown closed loop system. As the dc-link voltage V_{dc} was controlled in the dc–ac seven level PWM inverter, the change of the duty cycle changes the voltage at the output of the PV panels. A PID controller was implemented to keep the output voltage of the dc–dc boost converter (V_{dc}) constant by comparing V_{dc} and

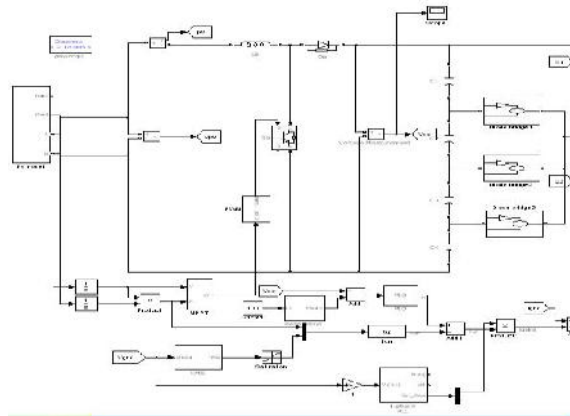


Fig.3. simulation circuit of Nine-level inverter with closed-loop algorithm

V_{dc} ref and feeding the error into the PID controller, which subsequently tries to reduce the error. In this way, the V_{dc} can be maintained at a constant value and at more than $\sqrt{2}$ of V_{grid} to inject power into the grid. To deliver energy to the grid, the frequency and phase of the PV inverter must equal those of the grid; therefore, a grid synchronization method is needed. The sine lookup table that generates reference current must be brought into phase with the grid voltage (V_{grid}). For this, the grid period and phase must be detected. The proposed inverter provides an analog zero-crossing detection circuit on one of its input ports where the grid voltage is to be connected. The zero-crossing circuit then produces an in-phase square-wave output that is fed into the digital I/O port on eZdsp board TMS320F2812. A PI algorithm was used as the feedback current controller for the application. The current injected into the grid, also known as grid current I_{grid} , was sensed and fed back to a comparator that compared it with the reference current $I_{gridref}$. $I_{gridref}$ is the result of the MPPT algorithm. The error from the comparison process of I_{grid} and $I_{gridref}$ was fed into the PI controller. The output of the PI

controller, also known as V_{ref} , goes through an anti windup process before being compared with the triangular wave to produce the switching signals for S1–S7. Eventually, V_{ref} becomes V_{ref1} ; V_{ref2} ; V_{ref3} and V_{ref4} can be derived from V_{ref1} by shifting the offset value, which was equivalent to the amplitude of the triangular wave.

V SIMULATION RESULTS

MATLAB SIMULINK simulated the proposed configuration before it was physically implemented in a prototype. The PWM switching patterns were generated by comparing three reference signals (V_{ref1} , V_{ref2} , V_{ref3} , and V_{ref4}) against a triangular carrier signal. Subsequently, the comparing process produced PWM switching signals for switches S1–S7, as. One leg of the inverter operated at a high switching rate that was equivalent to the frequency of the carrier signal, while the other leg operated at the rate of the fundamental frequency (i.e., 50 Hz). Switches S5 and S6 also operated at the rate of the carrier signal. Inverter output voltage (V_{inv}). Fig.10. shows Grid voltage (V_{grid}) and grid current (I_{grid}) of the carrier signal. Fig.9. shows the simulation result of inverter output voltage V_{inv} . The dc-bus voltage was set at 300 V ($>\sqrt{2}V_{grid}$; in this case, V_{grid} was 120 V). The dc-bus voltage must always be higher than $\sqrt{2}$ of V_{grid} to inject current into the grid, or current will be injected from the grid into the inverter. Therefore, operation is recommended to be between $M_a = 0.66$ and $M_a = 1.0$. Fig.5-8. Shows PWM signals for S1 to S7 switches. V_{inv} comprises seven voltage levels, namely, V_{dc} , $3V_{dc}/4$, $V_{dc}/2$, $V_{dc}/4$, 0, $-V_{dc}$, $-3V_{dc}/4$, $-V_{dc}/2$, and $V_{dc}/4$. The current flowing into the grid was filtered to resemble a pure sine wave in phase with the grid voltage see Fig. 10). As I_{grid} is almost a pure sine wave at unity power factor, the total harmonic distortion (THD) can be reduced compared with the THD.

Fig.4. Simulink output of PWM switching signal generation.

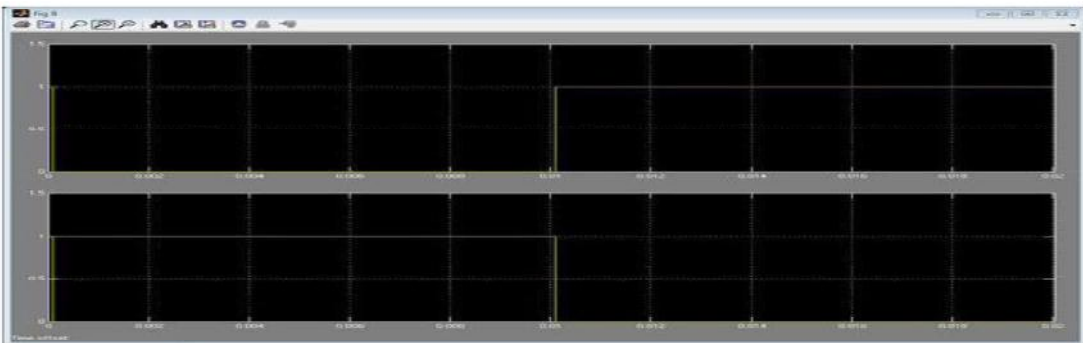
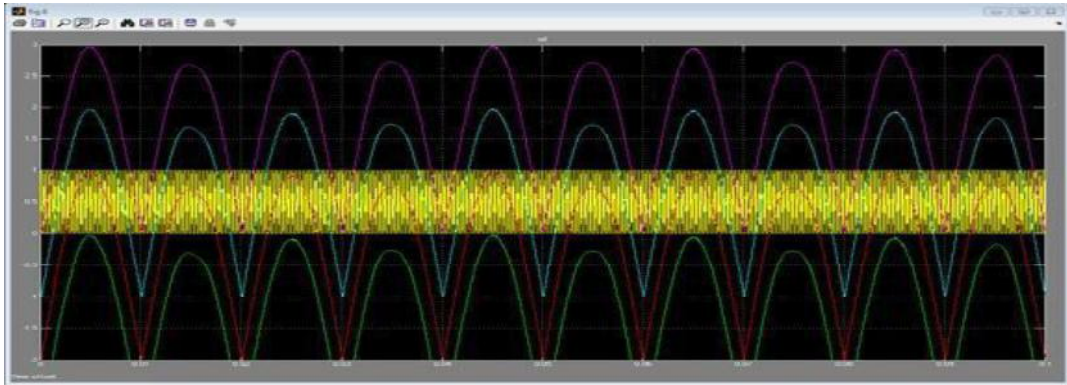


Fig.6. PWM signals for S2 and S4.

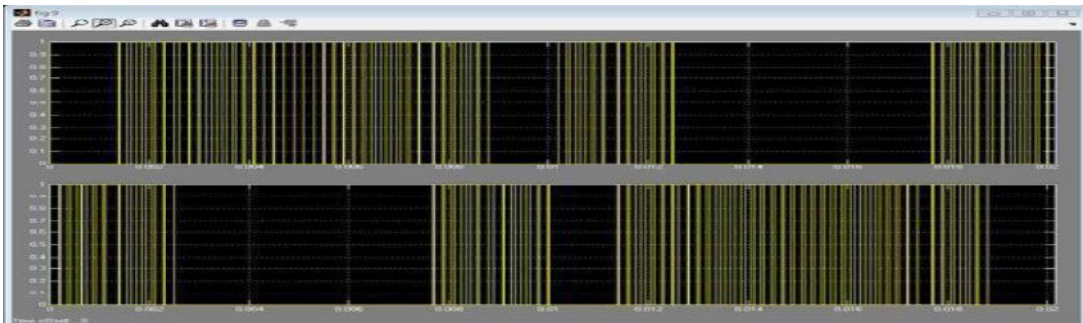


Fig.7. PWM signals for S5 and S6.

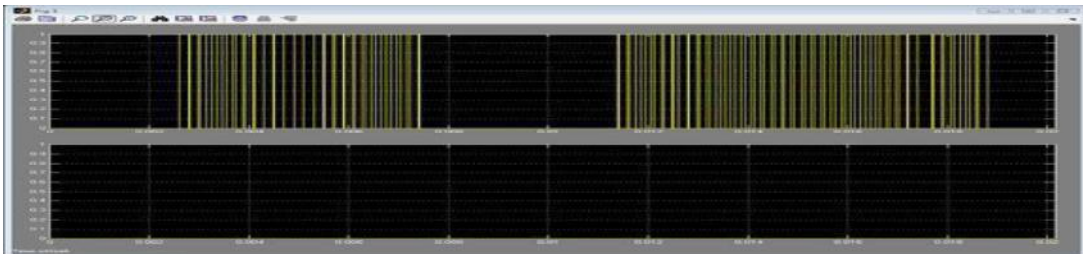


Fig.8. PWM signal for S7.

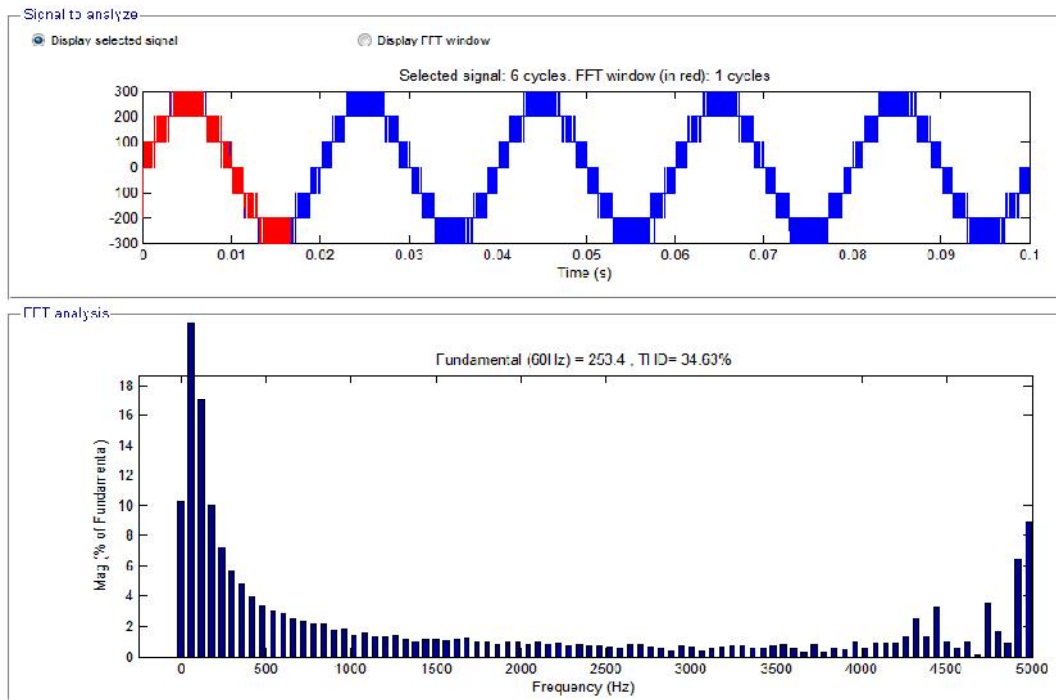


FIG: FFT for seven level Inverter

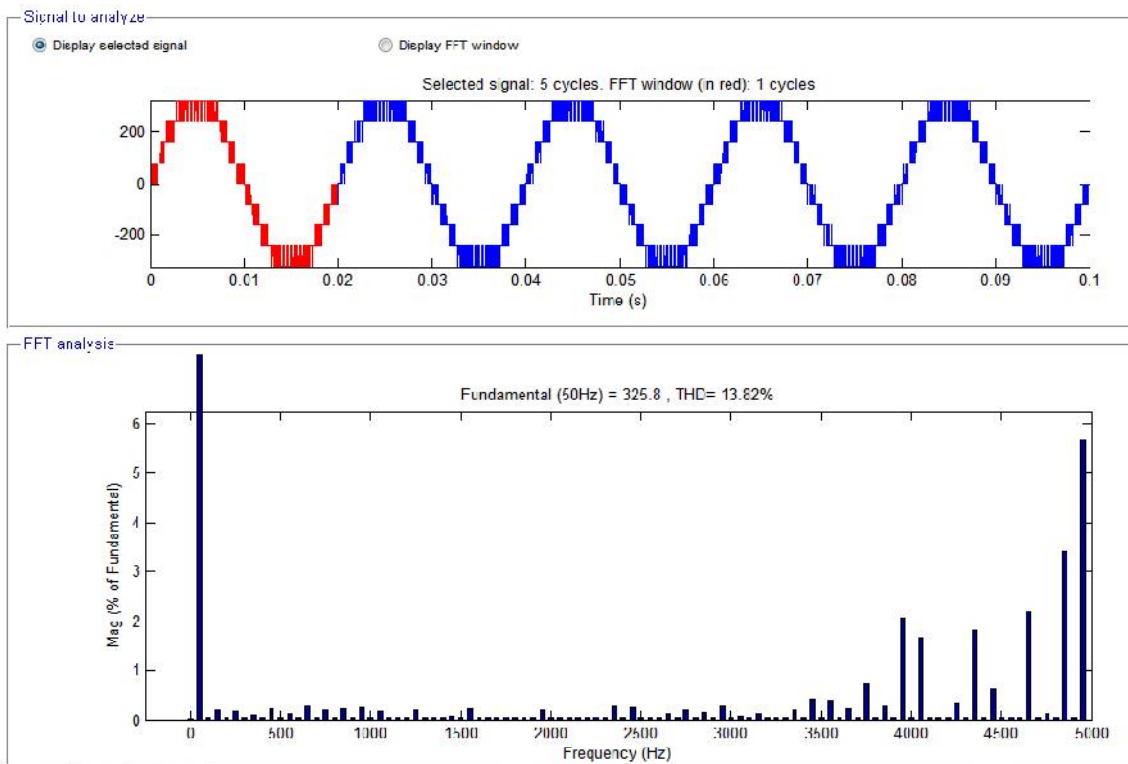


FIG: FFT for nine level Inverter

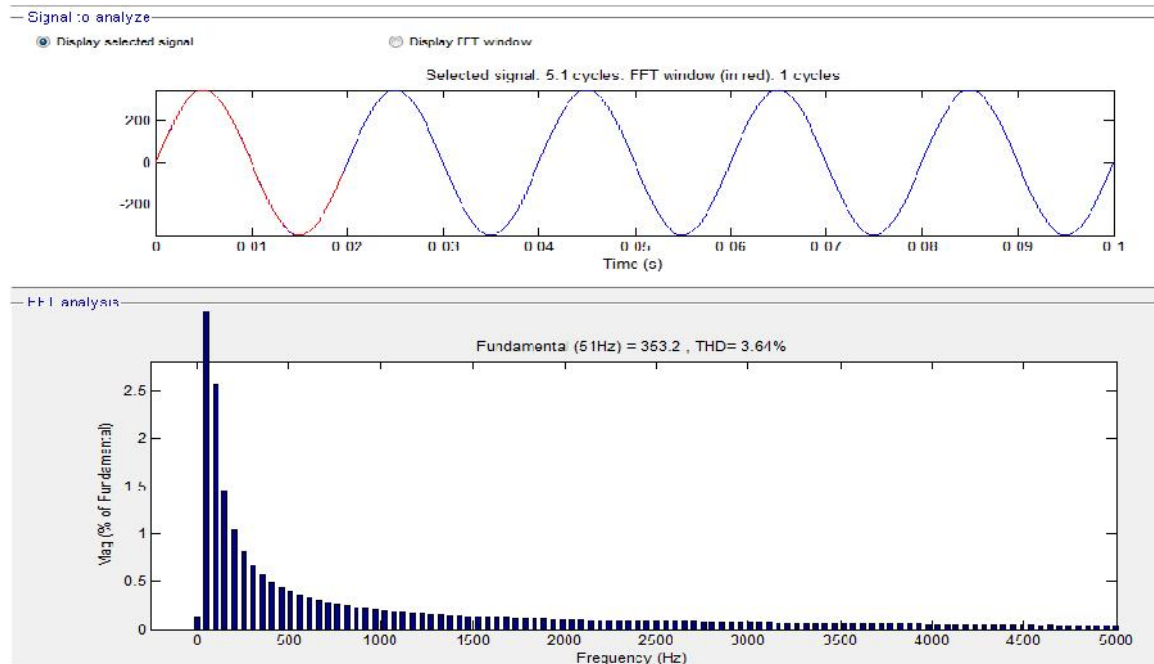


FIG: FFT at load side

VI. CONCLUSION

Multilevel inverters offer improved output waveforms and lower THD. This paper has presented a novel PWM switching scheme for the proposed multilevel inverter. It utilizes four reference signals and a triangular carrier signal to generate PWM switching signals. The behavior of the proposed multilevel inverter was analyzed in detail. By controlling the modulation index, the desired number of levels of the inverter’s output voltage can be achieved. Table 2 shows the less THD in the nine-level inverter compared with that in the seven-level, five-level and three level inverters is an attractive solution for grid-connected PV inverters.

REFERENCES

[1] M. Calais and V. G. Agelidis, —Multilevel converters for single-phase grid connected photovoltaic systems: an overview, in Proc. IEEE Int. Symp. Ind. Electron. 1998, vol. 1, pp. 224–229.
 [2] S. B. Kjaer, J. K. Pedersen, and F. Blaabjerg, —A review of single-phase grid connected inverters for photovoltaic modules, IEEE Trans. Ind. Appl., vol. 41, no. 5, pp. 1292–1306, Sep./Oct. 2005.
 [3] P. K. Hinga, T. Ohnishi, and T. Suzuki, —A new PWM inverter for photovoltaic power generation system, in Conf. Rec. IEEE Power Electron. Spec. Conf., 1994, pp. 391–395.
 [4] Y. Cheng, C. Qian, M. L. Crow, S. Pekarek, and S. Atcitty, —A comparison of diode-clamped and cascaded multilevel converters for a STATCOM with

energy storage, IEEE Trans. Ind. Electron., vol. 53, no. 5, pp. 1512–1521, Oct. 2006.
 [5] M. Saeedifard, R. Irvani, and J. Pou, —A space vector modulation strategy for a back-to-back five-level HVDC converter system, IEEE Trans. Ind. Electron., vol. 56, no. 2, pp. 452–466, Feb. 2009.
 [6] S. Alepuz, S. Busquets-Monge, J. Bordonau, J. A. M. Velasco, C. A. Silva, J. Pontt, and J. Rodríguez, —Control strategies based on symmetrical components for grid-connected converters under voltage dips, IEEE Trans. Ind. Electron., vol. 56, no. 6, pp. 2162–2173, Jun. 2009.
 [7] J. Rodríguez, J. S. Lai, and F. Z. Peng, —Multilevel inverters: A survey of topologies, controls, and applications, IEEE Trans. Ind. Electron., vol. 49, no. 4, pp. 724–738, Aug. 2002.
 [8] J. Rodríguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, —Multilevel voltage-source-converter topologies for industrial medium-voltage drives, IEEE Trans. Ind. Electron., vol. 54, no. 6, pp. 2930–2945, Dec. 2007.
 [9] M. M. Renge and H. M. Suryawanshi, —Five-level diode clamped inverter to eliminate common mode voltage and reduce dv/dt in medium voltage rating induction motor drives, IEEE Trans. Power Electron., vol. 23, no. 4, pp. 1598–1160, Jul. 2008.
 [10] E. Ozdemir, S. Ozdemir, and L. M. Tolbert, —Fundamental-frequency modulated Six-level diode-clamped multilevel inverter for three-phase Stand-alone photovoltaic system, IEEE Trans. Ind. Electron., vol. 56, No. 11, pp. 4407–4415, Nov. 2009.
 [11] R. Stala, S. Pirog, M. Baszynski, A. Mondzik, A. Penczek, J. Czekonski, and S. Gasiorek, —Results of investigation of multicell converters with balancing circuit—Part I, IEEE Trans. Ind. Electron., vol. 56, no. 7, pp. 2610–2619, Jul. 2009.

- [12] R. Stala, S. Pirog, M. Baszynski, A. Mondzik, A. Penczek, J. Czekonski, and S. Gasiorek, —Results of investigation of multicell converters with balancing circuit—Part II, IEEE Trans. Ind. Electron., vol. 56, no. 7, pp. 2620–2628, Jul. 2009.
- [13] P. Lezana, R. Aguilera, and D. E. Quevedo, —Model predictive control of an asymmetric flying capacitor converter, IEEE Trans. Ind. Electron., vol. 56, no. 6, pp. 1839–1846, Jun. 2009.
- [14] M. F. Escalante, J.-C. Vannier, and A. Arzandé, —Flying capacitor multilevel inverters and DTC motor drive applications, IEEE Trans. Ind. Electron., vol. 49, no. 4, pp. 809–815, Aug. 2002.
- [15] A. Shukla, A. Ghosh, and A. Joshi, —Static shunt and series compensations of an SMIB system using flying capacitor multilevel inverter, IEEE Trans. Power Del., vol. 20, no. 4, pp. 2613–2622, Oct. 2005.
- [16] J. Huang and K. A. Corzine, —Extended operation of flying capacitor multilevel inverter, IEEE Trans. Power Electron., vol. 21, no. 1, pp. 140–147, Jan. 2006.
- [17] F. Z. Peng, —A generalized multilevel inverter topology with self voltage balancing, IEEE Trans. Ind. Appl., vol. 37, no. 2, pp. 611–617, Mar./Apr. 2001.
- [18] E. Villanueva, P. Correa, J. Rodríguez, and M. Pacas, —Control of a singlephase cascaded H-bridge multilevel inverter for grid-connected photovoltaic

