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An Efficient Design of Low Power and Low Leakage Class-AB CMOS Amplifier using Gating Technique

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Abstract

A rail-to-rail class-AB CMOS buffer amplifier is proposed in this paper to drive large capacitive loads. A new technique is used to reduce the leakage power of class-AB CMOS buffer circuits without affecting dynamic power dissipation .The name of applied technique is Transistor Gating Technique, which gives the high speed buffer with the reduced low power dissipation , low leakage and reduced area also. The proposed buffer is simulated at 180nm CMOS technology and the circuit is operated at 1.65V supply with Cadence software. This analog circuit is performed with reduced performance degradation as well as high current driving capability for the large input voltages. The proposed paper is achieved very high speed with very low propagation delay.

Keywords: CMOS buffer, Class-AB, Rail-to-rail, Settling time, Slew-Rate, Transistor gating technique, Sleep transistor

1. Introduction

Today CMOS technology has been got more popularity than the bipolar technology especially for analogue circuits in to form the mixed signal systems. The industrial trend of this time wants to achieve the goal of minimum size of the chip. The most commonly used as amplifier is common emitter (Bipolar junction transistor) or common source (MOSFET) that magnifies and invert the input signal. Behzad Rajavi says that we know that MOSFET plays an important role in the reduced size of the chip, by reducing the gate oxide thickness of MOSFET *i.e.*, (T_{ox}). But reducing of the T_{ox} gives the reduced tolerance of the MOSFET devices for the higher voltage levels at the gate of MOSFET. It means that to reduce the maximum supply voltages V_{dd} it gives the helpful purpose. Due to the reduced supply voltages analogue designer have to face some common problems like input common mode range, output swing, and linearity of the device. In the resulting form to implement the desired analogue device we apply the CMOS technology with low voltage and low power techniques.

The second major aspect for the designers of analogue circuits is to stand the circuits with low power dissipation, which is helpful to improve the battery life of the electronic devices. As the CMOS technology is scaled down to the nanometers and femtometers the analogue circuitry has to need to maintain its quality of performance for many parameters like device size, bias currents, voltages, parasitic capacitances and the values of supply voltages. This scaled down feature of the CMOS technology and the reduced power dissipation is helpful to get the mixed mode type circuits, which is the combination of the analogue circuits and digital circuits.

Op-amps are the basic block of the analogue circuit, which are used in many applications like Digital-to-analog converters, RF receivers and transmitters. Op-amps are desired with some basic requirements such as low voltage supply, low power dissipation, rail-to-rail output swing, high slew rate, reduced settling time with the critical efficiency of power dissipation. These all requirements are necessary for portable electronics devices. As the op-amps, buffer amplifiers are also most important cell of the analogue circuits. Buffer amplifier also plays an important role in operational amplifier. Basically amplifiers are used for the amplification of the signals.

Amplifiers are mainly designed to amplify the input signal for voltage (voltage amplifier), for current (current amplifier) or for both types (power amplifier). An Amplifier performs operation with a single supply (*i.e.*, V_{dd} and Gnd) or with double sided supply (*i.e.*, V_{dd}, V_{ss} and Gnd). For the analogue systems operational amplifier (Op-amp) is a fundamental block. To achieve the high performance of Op- amp, which is based on the analogue circuits we have to consider some basic parameters for any op-amp. An Operational amplifier has many basic parameters. Some important parameters are given here such as slew rate, settling time, common mode range, frequency response, input offset voltage. These all parameters play an important role for any electronic circuit which is made up with the Op-amp.

Although the amplification of a Class A amplifier, (where the output transistor conducts 100% of the time) can be high, the efficiency of the conversion from the DC power supply to an AC power output is generally poor at less than 50%. However if we modify the Class A amplifier circuit to operate in Class B mode, (where each transistor conducts for only 50% of the time) the collector current flows in each transistor for only 180º of the cycle. The advantage here is that the DC-to-AC conversion efficiency is much higher at about 75%, but this Class B configuration results in distortion of the output signal which can be unacceptable.

One way to produce an amplifier with the high efficiency output of the Class B configuration along with the low distortion of the Class A configuration is to create an amplifier circuit which is a combination of the previous two classes resulting in a new type of amplifier circuit called a **Class AB Amplifier**. Then the Class AB amplifier output stage combines the advantages of the Class A amplifier and the Class B amplifier while minimizing the problems of low efficiency and distortion associated with them.

Class-AB buffer is also described already in background part. Class- AB buffer amplifiers are mostly used by MOS analogue circuitry. Class-AB amplifiers are mainly used for low power consumption and to gain reduced cross-over distortion.

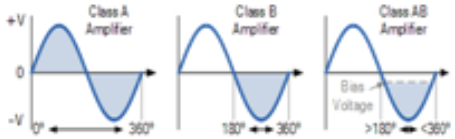

Figure 1. Comparison of Class A, B, AB Amplifier

The proposed paper is based on a new current leakage scheme. Buffer circuits are mostly used to run the large capacitive load at high speed. Here rail to rail class-AB CMOS buffer is presented to drive the large capacitive loads. Presented paper has the enhanced slew rate with the low power dissipation. This paper is based on the new leakage current technique *i.e.*, TRANSISTOR GATING. In the next section class-AB voltage buffer with its performance analysis is presented. Section II presents the new low power dissipation scheme. Section IV presents the proposed new high speed buffer. Section V has the simulation results of proposed buffer. And Section VI presents the conclusion of proposed buffer.

2. Class-AB Rail-to-Rail Buffer

Class-AB rail-to-rail buffer contains some common features are explained in the following sub-sections.

2.1. Rail-to-rail Input Swing

To achieve the rail-to-rail swing, an NMOS pair and an PMOS pair added in parallel configuration. The CMR voltage range of the n-channel pair is written as;

$$Vcmn \geq Vss + Vgsn + Vdsn \quad (1)$$

Where V_{gsn} and V_{dsn} are the gate-source voltage and drain-source voltage respectively.

Similarly, the CMR of p-channel pair is written as;

$$Vcmp \leq Vdd + Vgsp + Vdsp \quad (2)$$

To get rail-to-rail input range, one or both pair should be in "active mode", which requires

$$Vcmp-max \geq Vcmn-min \quad (3)$$

Put the equation (1) and (2) in equation (3)

$$Vdd-Vss \geq Vgsp+Vdsp+Vgsn+Vdsn \geq 2Vth \quad (4)$$

Here equation (4) shows that V_{th} of NMOS and PMOS are same, and then the value of applied voltage should be higher than twice of the threshold voltage V_{th} of the applied technology.

2.2. Class-AB Buffer

Class-AB buffer is mostly used to reduce the tradeoff between speed characteristics and power dissipation. The function of class-AB buffer is also called the adaptive biasing. Adaptive biasing is useful to improve the slew rate performance. To achieve this phenomenon we need high quiescent current so, that power - consumption will also increase. To remove this contradiction Transistor gating technique is applied.

In class- AB operation, each device operates the same way as in class-B over half the waveform, but on the same side it also conducts a small amount on the other half. As per result the region where both devices simultaneously are nearly off (the dead zone) is reduced. According to the result when the waveform from the two devices are combined, the crossover greatly minimized or eliminated altogether .The exact choice of quiescent current, the standing current across both devices when there is no signal, then it make a large difference at the level of distortion (and to the risk of thermal run away, that may damage the devices) often the bias voltage applied to set this quiescent current has to be adjusted with the temperature of the output transistor.

Figure 2. Class AB Amplifier Schematic

2.3. Power Consumption of Circuit

As we know that any CMOS circuit has the power dissipation in the standby mode which is two types static and dynamic dissipation. When the transistors go to switching condition then dynamic power is consumed by the transistors. Some main components of the static power dissipation are given as junction leakage, Sub-threshold leakage, and gate oxide leakage. In the standby mode of the circuit, the static power dissipation is given by equation $P_L = I_L \times Vdd$

Where P_L is leakage power of the transistor, I_L is leakage current of the transistor in off state of the transistor. And Vdd is supply voltage. Here various components are contained by leakage current. The gate leakage and sub-threshold leakage are main leakage in the given leakages such as sub-threshold leakage, gate leakage, reverse biased junction leakage and gate induced drain leakage.

The sub-threshold leakage current of MOS transistor is given in equation (6) and (7)

$$I_{ds} = I_{dso} e \text{ ^}[(V_{gs}-V_t)/nvT]* [1 - e\text{^}V_{ds}\ V_T] \quad (6)$$

$$I_{dso}=\mu_{eff} C_{ox}(W|L)V_T^2 \quad (7)$$

Where μ_{eff} is the charge carrier mobility, C_{ox} is the gate capacitance per unit area, W is width and L is length of channel of transistor, V_t is threshold voltage, vT is the thermal voltage, n is the sub- threshold swing coefficient, V_{gs} is the transistor gate to source voltage and V_{ds} is drain to source voltage.

3. Low Power Dissipation Scheme for CMOS Buffer

The power dissipation is an important consideration in the CMOS VLSI design circuits. High power consumption leads to reduction in the battery life-, in the case of battery-powers applications and in reliability, packaging and cooling costs. **The main sources of power dissipation are:** (a) capacitive power dissipation. (b) Short circuit currents. (c) Leakage currents. In CMOS technology leakage power occurs due to the sub-threshold which is the reverse current flowing through the off transistor. Gate leakage is also another type of leakage. The feature size and the channel length of transistor are reducing day by day, because the technology is also scaled down. Due to decrement in the channel length we get the increment of the leakage power in the total dissipated power.

3.1 Gating Technique:

Fig 3 shows the block diagram of transistor GATING TECHNIQUE, which has the advantage of low leakage current of the buffer circuit which is achieved after the simulation of the circuit at cadence software.

This technique has two sleep transistor PMOS and NMOS which are used in circuit. Here sleep transistor PMOS (S) is inserted between the pull-up network and network outputs and sleep transistor NMOS (S') is inserted between the pull-down network and ground to reduce the leakage current. During active mode by applying proper gate input

voltage both transistor will get on position *i.e.*, high for NMOS and low for PMOS. It is helpful to reduce the resistance of conducting path from power supply to ground, which gives the reduced performance degradation.

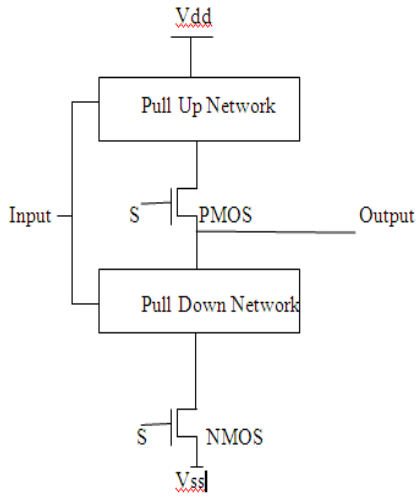

Figure 3. Gating Technique

From the above theory the gate leakage and sub-threshold are main leakages, that type of leakages can be reduces by help of the transistor GATING TECHNIQUE. During standby mode, by applying proper gate input both sleep transistors will get turn off position *i.e.* , low for NMOS and high for PMOS to produces the stacking effect, which reduce leakage current by increasing resistance of the path from power supply to ground. By help of this phenomenon an additional resistance is provided which decreases the sub-threshold leakage current.

4. Simulation Results

Using 180nm CMOS technology we designed a new buffer as shown in Figure 4, which is simulated at 1.65V supply voltage by help of the cadence tool. Figure 3 consists the transistors that all have the same sizing. Bias current I_B is fixed at 10μA in buffer circuit. It contains the 10pF capacitor, fixed at the output side. Figure 5 shows the input and output waveform. And Figure 6 shows the Gain versus Phase response waveform of the buffer circuit.

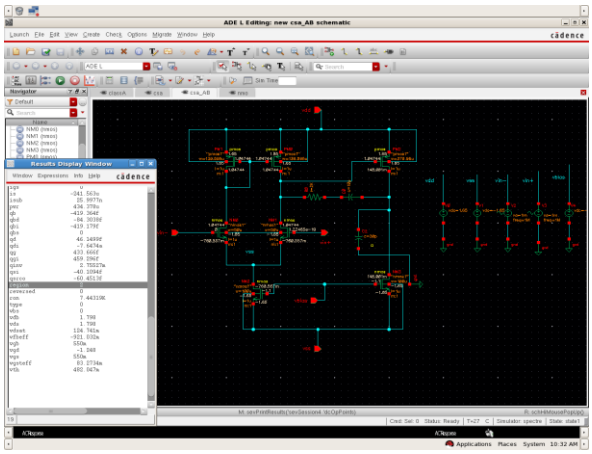

Figure 4: DC Analysis of Class AB

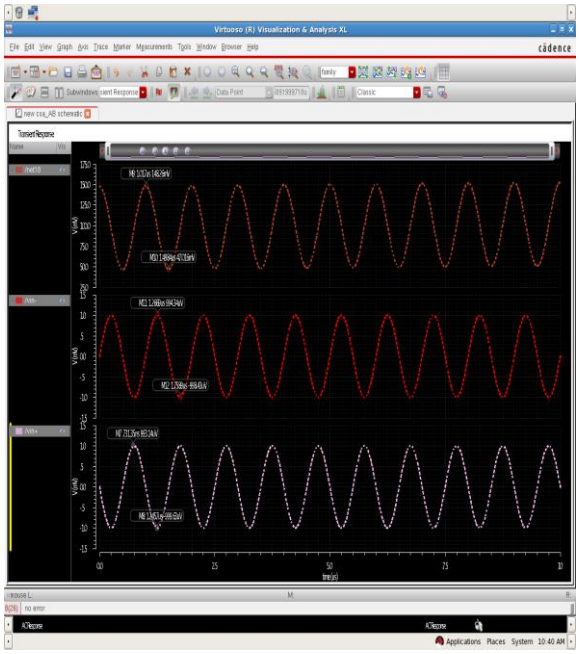

Figure**5:** Transient Analysis-I/O Waveform

Figure6: AC Gain and Phase Response- Max Gain=91dB

5. Conclusion

A new design scheme for CMOS class-AB buffer using the TRANSISTOR GATING technique is proposed. By help of this technique reduced leakage current is achieved. Applying the TRANSISTOR GATING technique with the adaptive biasing into the buffer helped us to get the propagation delay in the range of Pico - seconds i.e.345.1×10 -12, from here we can concluded that the speed of this buffer is very high. The settling time of proposed circuit is also reduced to the range of nanoseconds. This technique is also capable to enhance the slew rate, the achieved slew rate is 90(V/μs).The designed buffers is applicable in systems requiring the efficient operation with very low quiescent power consumption.

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