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RECENT ADVANCES IN ELECTRONICS & COMMUNICATION ENGINEERING (RAECE-2K17)

Braun's Multiplier Implementation using Ripple Carry Adder, Kogge-Stone Adder and 14-transistor novel ADDER.

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ABSTRACT:
Developing an Application Specific Integrated Circuits (ASIC‟s) willcost very high, circuits should be proved and then it would be optimized before implementation. Multiplication, which is the basic building block for several DSP processors[7], Image processing and many other , can be easily done by the implementation of Braun‟s Multiplier using different Adder Cells. The implementation of this multiplier and its bypassing techniques is done using Cadence(Back End). There is the reduction in the factors like delay LUT‟s, number of slices used. The Braun‟s Multiplier uses the full adder block and fast addition method so that we are reducing the delay. In the Row and Column bypassing method we used ripple carry adder, kogge-stone adder and 14-transistor novel adder. The structure consists of array of AND gates and adders arranged in the iterative manner. The proposed system "BRAUN‟S MULTIPLIER IMPLEMENTATION USING RIPPLE CARRY ADDER, KOGGE STONE ADDER AND 14-TRANSISTOR NOVEL ADDER" is implemented in 45nm technology using cadence virtuoso tool. The circuit schematic designed and the circuits are simulated for functionality verification.

Key words:
Digital Signal Processing (DSP), Braun‟s multiplier, fast addition, Kogge-Stone adder.

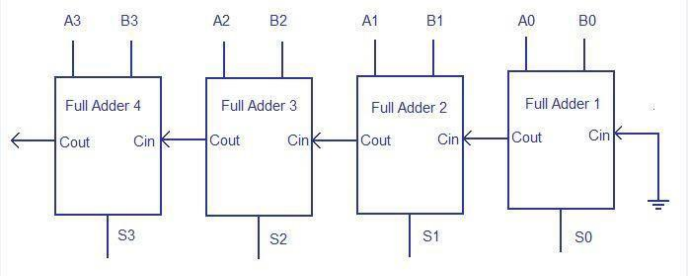
INTRODUCTION

Multiplication – an important fundamental function in arithmetic operation. Currently implemented in many DSP applications such as FFT, Filtering etc., and usually contribute significantly to time delay and take up a great deal of silicon area in DSP system[7]. Now – a – days time is still an important issue for the determination of the instruction cycle time of the DSP chip. Both the multiplication and the DSP play a vital role in the implementation of VLSI system[6]. Multiplication – Repeated addition of n – bits will give the solution for the multiplication. ie. Multi-operand addition process. The multi – operand addition process needs two n – bit operands. It can be realized in n- cycles of shifting and adding. This can be performed by using parallel or serial methods. This will be simple to implement in two‟s complement representation, since they are independent of the signs. It is advantageous to exploit other number systems to improve speed and reduce the chip area and power consumption. Generally multiplications can be carried out in all the types of number

system. The one which carried out for the Binary number system is the Digital multiplier.

RIPPLE CARRY ADDER

Multiple full adder circuits can be cascaded in parallel to add an N-bit number. For an N- bit parallel adder, there must be N number of full adder circuits. A ripple carry adder is a logic circuit in which the carry-out of each full adder is the carry in of the succeeding next most significant full adder. It is called a ripple carry adder because each carry bit gets rippled into the next stage. In a ripple carry adder the sum and carry out bits of any half adder stage is not valid until the carry in of that stage occurs. Propagation delays inside the logic circuitry is the reason behind this. Propagation delay is time elapsed between the application of an input and occurrence of the corresponding output. Consider a NOT gate, When the input is "0" the output will be "1" and vice versa. The time taken for the NOT gate"s output to become "0" after the application of logic "1" to the NOT gate"s input is the propagation delay here. Similarly the carry propagation delay is the time elapsed between the application of the carry in signal and the occurrence of the carry out (Cout) signal. Circuit diagram of a 4-bit ripple carry adder is shown below.



Sum out S0 and carry out C out of the Full Adder 1 is valid only after the propagation delay of Full Adder 1. In the same way, Sum out S3 of the Full Adder 4 is valid only after the joint propagation delays of Full Adder 1 to Full Adder 4. In simple words, the final result of the ripple carry adder is valid only after the joint propagation delays of all full adder circuits inside it.

Preprocessing is the first stage where the generate and propagate signals of all the input pairs of signals A and B are generated individually for each bit. The logical equations of the propagate and generate signals are given by the following equations:

Carry generation network :

Carry generation is the second stage of the KSA. At this stage the carries of all the bits are generated individually for each bit. They are divided into slighter pieces and this overall method is carried out in parallel for all the bits. Carry generate and Carry propagate bits are used as midway signals and their logical equations are given as follows:

CPi:j = Pi:k + 1 and Pk:j

CGi:j = Gi:k + 1 or (Pi:k + Gk:j)

Post processing stage :

This is the final step or last stage of the KSA which is general for all types of adders, i.e., calculation of summation of the bits given by the logical equations,

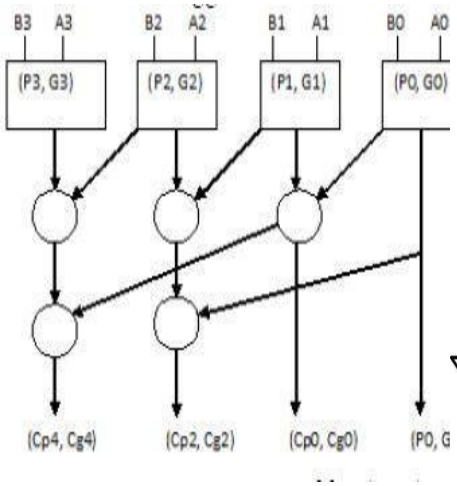


Fig.2. 4 bit Kogge Stone Adder

14-Transistor novel adder:

The 14-transistor novel adder[5] is a modified version of the conventional full adder. The novel adder consists of 14 transistors only, which reduce the delay when compared with the normal full adder.

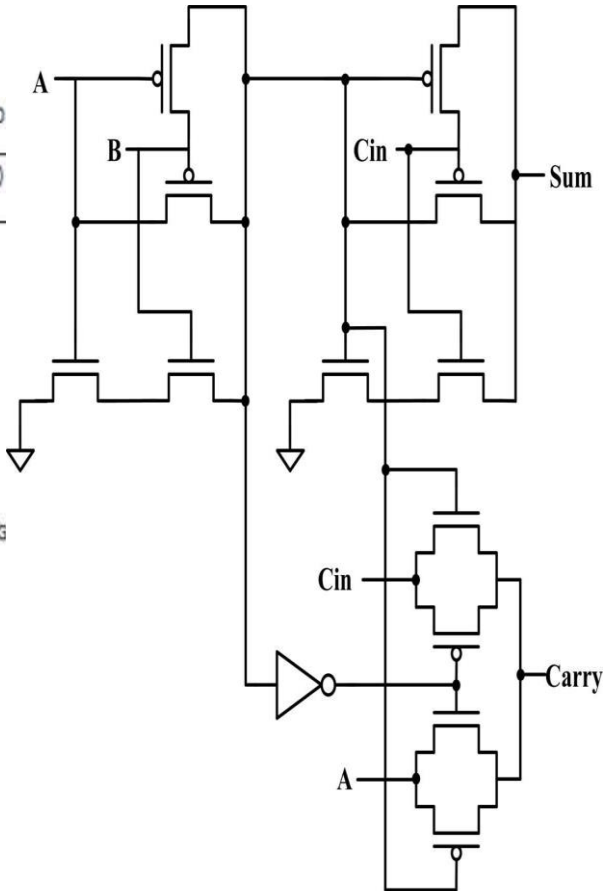


Fig 3. 14-Transistor Novel Full Adder

BRAUN MULTIPLIERS:

It is a simple parallel multiplier generally called as carry save array multiplier. It has been restricted to perform signed bits. The structure consists of array of AND gates and adders arranged in the iterative manner and no need of logic registers. This can be called as non – addictive multipliers.

Architecture:

An n*n bit Braun multiplier is constructed with n (n-1) adders and n2 AND gates as shown in the fig.4, where,

X: 4-bit multiplicand
Y: 4-bit multiplier
P: 8-bit product of X and Y
$P_n = X_iY_j$ is a product bit

The internal structure of the full adder can be realized using FPGA. Each products can be generated in parallel with the AND gates. Each partial product can be added with the sum of partial product which has previously produced by using the row of adders. The carry out will be shifted one bit to the left or right and then it will be added to the sum which is generated by the first adder and the newly generated partial product.

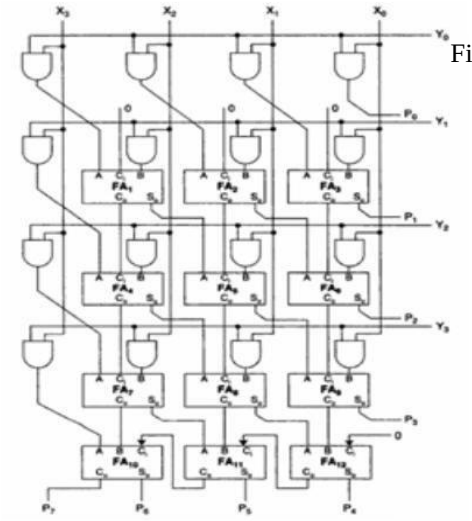


Fig.4 Braun"s Multiplier.

The shifting would carry out with the help of Carry Save Adder (CSA) and the Ripple carry adder should be used for the final stage of the output. Braun multiplier performs well for the unsigned operands that are less than 16 bits in terms of speed, power and area. But it is simple structure when compared to the other multipliers. The main drawback of this multiplier is that the potential susceptibility of Glitching problem due to the Ripple Carry Adder in the last stage. The delay depends on the delay of the Full Adder and also a final adder in the last. The power and area can also be reduced by using two bypassing techniques called **Row bypassing technique (fig. 5) [4& 3]** and **Column bypassing technique (fig. 6) [4]** and **Row and column bypassing technique (fig. 7).**

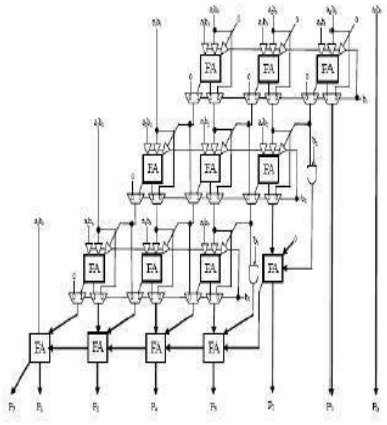


Fig. 5 4*4 row bypassing

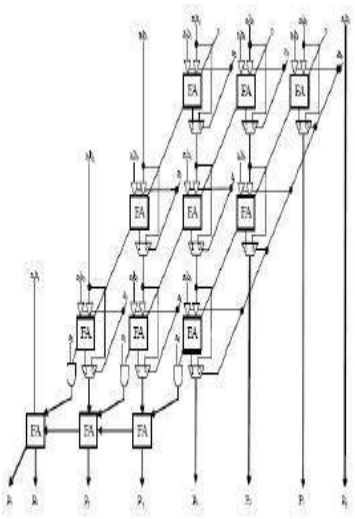


Fig. 6 4*4 column bypassing

TWO DIMENSION BYPASSING TECHNIQUE

The modified Adder cell in two-dimensional bypassing[1] consists of a FA, 3 tri-state buffers, two 2-to-1 mux and an extra AND gate at the carry output of the FA as shown. To correct the carry propagation in the multiplication result, the addition operations in the (i+1)th column or the jth row cannot be bypassed if the bit ai is 0, the bit bj is 0, and the carry bit, ci,j-1, is 1. Hence, the bypass logics are added into the necessary FA to form a correct adder cell (AC).

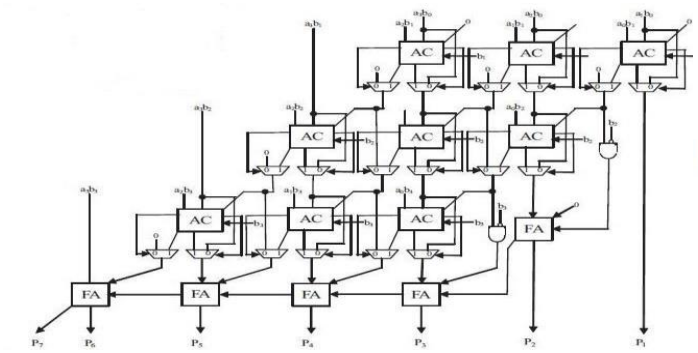


Fig. 7 4*4 row and column bypassing

USING KOGGE STONE ADDER

Bypassing means turning off some Rows or Columns when their outputs are known. This operation is performed when multiplier or multiplicand or both bits are low. It reduces the switching activities and thus power can be saved. 4/8/16 bit Row Bypassing, Column bypassing and Row and Column based Braun multiplier is implemented by using KSA. In 4/8/16 bit Row bypassing technique 4/8/16 bit KSA is required respectively. In 4/8/16 bit Column and mixed (Row and Column) bypassing technique 3/7/15 bit KSA is required. Here 4 bit Row, Column and Mixed bypassing using KSA[2] is shown as below

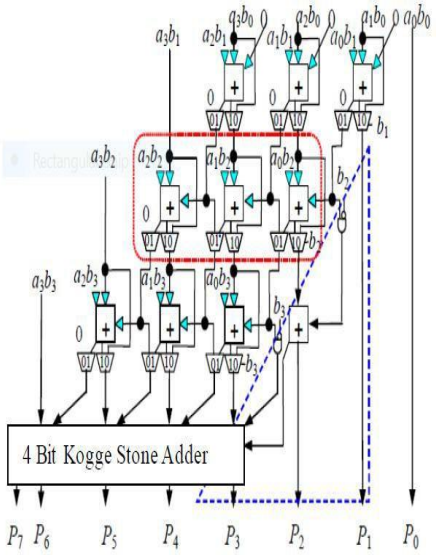


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Fig. No. 8. A 4*4 Braun Multiplier with Row Bypassing Using KSA

USING 14 transistor adder:(proposed system)

The modified Adder cell in two-dimensional bypassing consists of a FA, 3 tri-state buffers, two 2-to-1 mux and an extra AND gate at the carry output of the FA as

shown in fig 9. To correct the carry propagation in the multiplication result, the addition operations in the (i+1)th column or the jth row cannot be bypassed if the bit ai is 0, the bit bj is 0, and the carry bit, ci,j-1, is 1. Hence, the bypass logics are added into the necessary FA to form a correct adder cell (AC). The final stage consists of the 14 transistor adder cell.

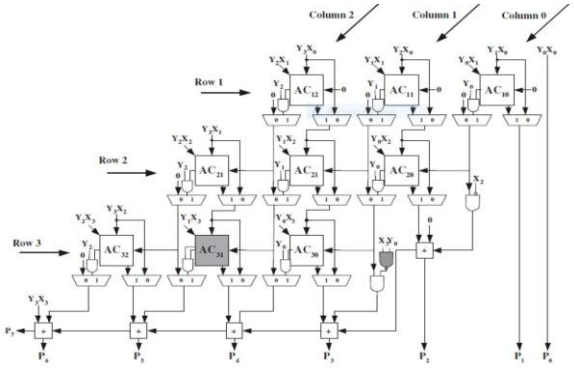

Fig. No. 9. Braun‟s Multiplier using 14 transistor adder.

COMPARISON :

The braun‟s multiplier is implemented by using ripple carry adder and kogge-stone adder the final stage in multiplier is changed. The 14-transistor novel adder uses full adders in all stages . From the implementation we achieved the below values which implies,

Power :

Brauns multiplier using 14t adder > Brauns multiplier using kogge-stone adder > Brauns multiplier using Ripple carry adder.

Delay:

Brauns multiplier using 14t adder < Brauns multiplier using kogge-stone adder < Brauns multiplier using Ripple carry adder.

S. No	Circuit	Power	Critical Delay
1	Brauns multiplier using RCA	10.33uw	143.9ps
2	Brauns multiplier using KSA	17.22uw	117.7ps
3	Brauns multiplier using 14t adder	1.716mw	56.52fs

Conclusion:

In this paper we have presented the hardware implementation of the Multipliers in the Cadence backend design. The design was implemented on Cadence 45nm technology. The proposed Multiplier shows that reduced utilization when compare to all other multipliers. The average pin delay and combinational path delay has been reduced . And it is feasible for the DSP Processor, Image processing and multimedia technology. We suggest the 14-transistor novel adder can be used in the DSP processors to increase the performance.

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