INTERNATIONAL JOURNAL OF RECENT TRENDS IN ENGINEERING & RESEARCH
Impact Factor 4.101 ISSN -2455-1457
RECENT ADVANCES IN ELECTRONICS & COMMUNICATION ENGINEERING (RAECE-2K17)

Design and Analysis of Carry Look Ahead Adder using 180nm Technology

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ABSTRACT:- **Addition forms the basic structure for digital signal processing operations like counting, multiplication, filtering etc. Adder circuits perform addition of two binary numbers which is a great interest for many designers in arithmetic logic unit. Compare with Ripple carry adder, Carry-look ahead adder has advantage in processing speed, so carry-look ahead adder is a major functional block in arithmetic logic unit due to its high speed operation. Therefore, it is of interest to study the functional behaviour and power consumption of carry-look ahead adder. In this project, the proposed adder has been designed by using 180 nm STATIC CMOS technology and founded that static CMOS logic offers low delay compare with adiabatic logic which offers low power.**

KEYWORDS**: 8TCircuit, XNOR Circuit, Generate, Propagate.**

I. Introduction

ALU is the fundamental building block in central processing unit. It needs adder circuit for addition and multiplication. Now a day, Power, Area and Speed are playing a major performance parameters for VLSI designer.

Binary addition is a popular methodology among computational logic elements. There are lots of ways of implementing the binary addition. Encoding, replication of common factors and pre-charging are some of them. Any functional block can be implemented using different logic approach like static, CMOS, dynamic logic, pass transistor based logic and adiabatic logic etc. Each Logic is having its own advantage based on simplicity, in terms of area that is related to cost, delay and power consumption. The n-bit ripple carry adder has n one-bit full adders. In this method the carry is computed. The addition is not complete until the n-1th adder has computed the n-1th output. The total delay of the logic element is due to the carry chain. Therefore, speeding up the adder needs the speeding up the carry chain. As speed of the addition is the main criteria, the carry look ahead adder has been chosen.

Now we have to design a carry look ahead adder by implementing our own technique such that functional behaviour of the circuit should be correct but off course by keeping in mind the design constraints like AREA as well as POWER as these are our concern. Layout is the final implementation of the circuit and circuit is just symbolic representation to achieve less transistor count. This can be done by using STATIC CMOS logic Style. So, we have designed carry look ahead adder by using STATIC CMOS logic style.

II. Related Work

Proposed Carry look ahead adder designed by using Static style and the Technology used is 180nm and has Low Area and Low Power. We have used NOR, NAND, XNOR and 8T Circuit as our Building blocks and their Maximum Fan-in is 3, Maximum Fan-out is 4 and the Design was developed at Transistor level which can give maximum Optimization since it is the Lowest level of Design abstraction.

III. Carry Look Ahead Adder

Adder is going to add 4 bits of A (A3 to A0) and 4 bits of B (B3 to B0) and gives 5-bit result out of them 4-bits will be sum bits and 1-bit will be carry bit. We can design the circuit for Carry look ahead adder which by default gives high speed but at the cost of Area. Fig.1 shows the block diagram of 4bit CLA

Now we can design the circuit for 4-bit carry look ahead adder coming from the least significant bit side that is A0 and B0, there will be Carry in. Now just a Xnor circuit is needed and it is a Two-Output Circuit in which first output is the Propagate output (p0) and second is the Generate output (G0). To achieve Propagate and Generate for the rest of bits that is P1, G1, P2, G2, P3, G3 Xnor circuit can be again used and now we are with all Generate and Propagate outputs. Now to find out Carry output of Least Significant Bit that is c1, two 2-input Nand gates are require. Now to find out Carry output of (Least Significant+1) Bit that is c2 we require three 2-input Nor gates and one 2-input Nand gate. Now to find out Carry output of (Least Significant+2) Bit that is c3 we require two not gates, three 2-input Nor gates, one 3input Nor gate and one 2-input Nand gate. Now to find out Carry output of Most Significant Bit that is c4, one 8TCircuit is required.

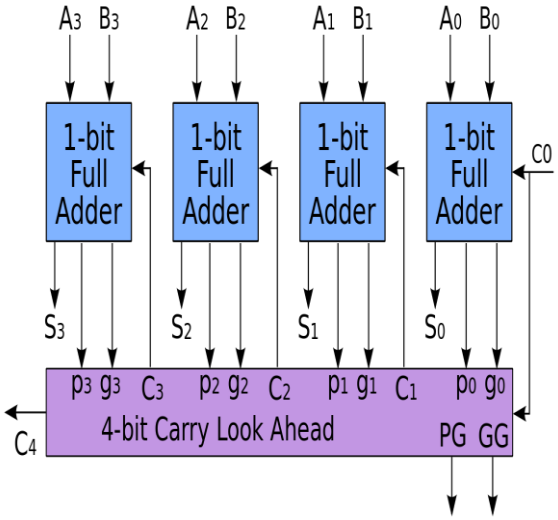

Fig.1 Block Diagram of 4bit CLA

Now to find out Sum output of Least Significant Bit that is S0, one 2-input Xnor gate is required. Now to find out Sum output of (Least Significant+1) Bit that is S1 we require one 2-input Xnor gate. Now to find out Sum output of (Least Significant+2) Bit that is S2 we require one 2-input Xnor gate. Now to find out Sum output of Most Significant Bit that is S3 we require one 2-input Xnor gate.

XNOR, 8T Circuit are 2 cells named in this Carry look ahead adder. XNOR has two inputs and two outputs and it takes 10 numbers of Transistors, 8T Circuit has four inputs and one output and needs 8 numbers of Transistors. Fig.2 shows an 8TCircuit which has four inputs and one output and it was needed to calculate the final Carry that is C4. Fig.3 shows a XNOR Circuit which has two inputs and two outputs and it was needed to find out the Generate and Propagate Outputs.

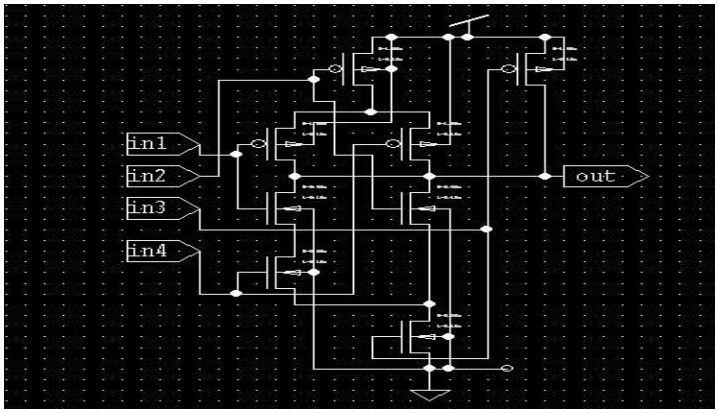

Fig.2 8Transistor Circuit

Fig.2 shows an 8Transistor Circuit which has four inputs and one output and it was needed to calculate the final Carry that is C4. Out of the four inputs input2 gives the Propagate Output of the MSB bits, input3 gives the Generate Output of the MSB bits, remaining are the previous Propagate and Generate Outputs. We can clearly Observe when Input3 is activated Low Output will be High.

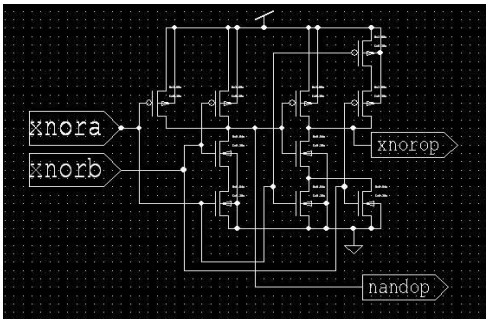

Fig.3 XNOR Circuit

Fig.3 shows a XNOR Circuit which has two inputs and two outputs and it was needed to find out the Generate and Propagate Outputs. Generate Output is Designed for Low and Propagate Output is also the same. This block is needed at every bit position from MSB to LSB

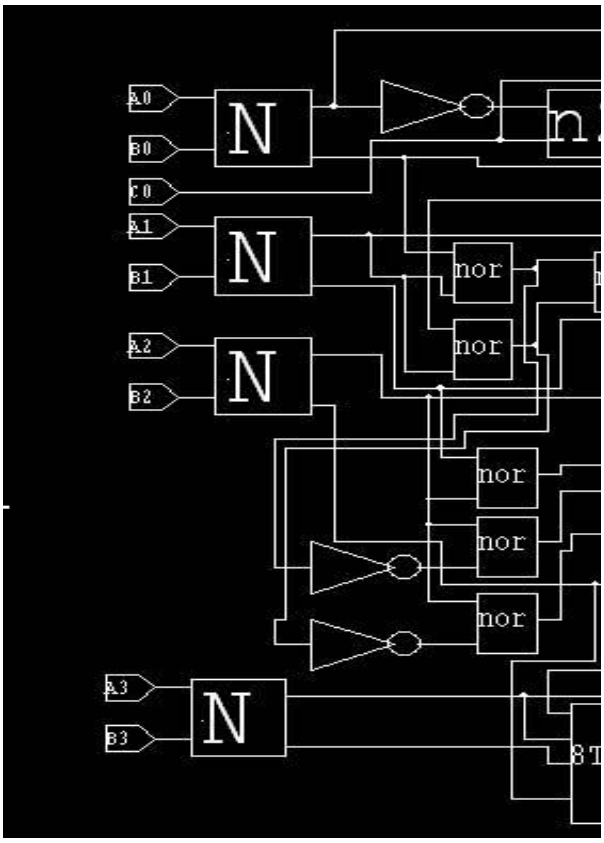

Fig.4 4-bit CLA Schematic diagram

Fig.4 shows a 4-bit CLA Circuit which has nine inputs and eight outputs out of which four are Sum and four are Carry Outputs. It consists of three not gates, one 8TCircuit, four 2-input Nand (N2) gates, one 3-input Nor gate, 6 two-input Nor gates and eight two-input Xnor gates. Total Transistor count is 140.

IV. Simulation Results

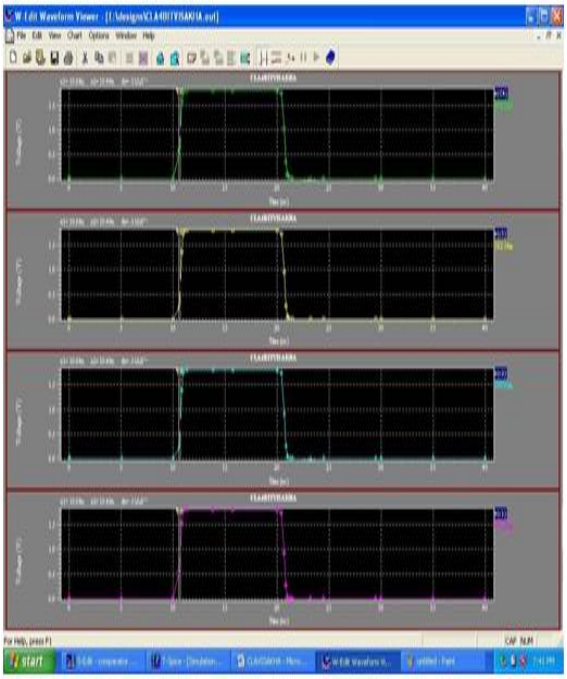

Fig.5 Delays for Low to High Carry outputs.

Fig.5 shows Delay comparisons of all the Carry Outputs C1, C2, C3 and C4. The worst Delay is for C4 and it is 0.14ns. It has been observed that Delay difference between all the Carry Outputs is less. Above Waveform has two Vertical Cursor Bars and the first one corresponds to Input changing 50% and Second one corresponds to Output changing 50%. Second Vertical Cursor Bar of C4 depicts Output reaching 0.9 volts.

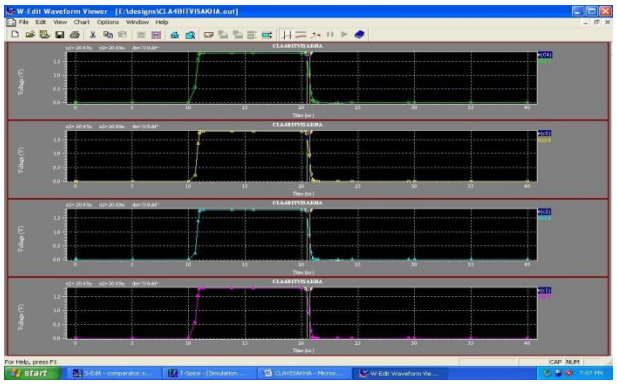

Fig.6 Delays for High to Low Carry outputs

Fig.6 shows Delay comparisons of all the Carry Outputs C1, C2, C3 and C4. The worst Delay is for C4 and it is 0.19ns. So the final Delay is the average of High to Low and Low to High Delays and it is 0.165ns. It has been observed that Delay difference between all the Carry Outputs is less.

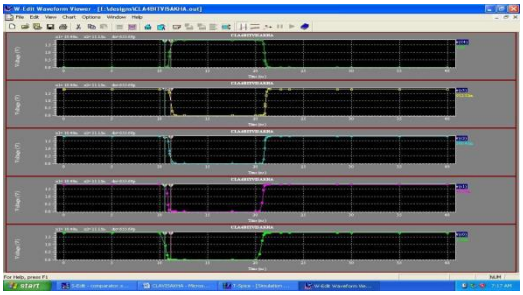

Fig.7 Delays for High to Low Sum outputs.

Fig.7 shows Delay comparisons between Sum outputs and the worst Delay is for S3 and it is 0.65ns.It has been observed that Delay difference between all the Sum Outputs is less. Vertical Cursor Bars are placed at the Output Transition of '1' to '0'.

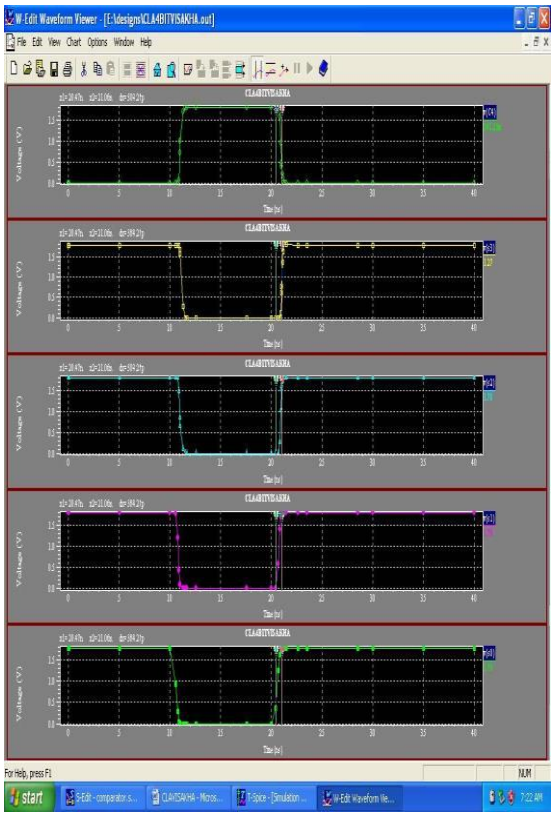

Fig.8 Delays for Low to High Sum outputs.

Fig. 8 shows Delay comparisons between Sum outputs and the worst Delay is for S3 and it is 0.56ns. It has been observed that Delay difference between all the Sum Outputs is less. Vertical Cursor Bars are placed at the Output Transition of '0' to '1'. So the final delay for Sum is 0.6ns.

V. **Performance Analysis**

Implementation of proposed 4-bit Carry look ahead adder has been done using STATIC CMOS logic style and it has been found that Carry look ahead adder has very less power dissipation in 56.8nW and requires only 140 number of Transistors for designing, resulting in less amount of area and in equal proportion reduction will be for N-bit.

VI. **Conclusion**

Carry look ahead adder is widely used where fast computation is needed especially in multipliers but disadvantage is Area will become worsen as size increases but we were able to design the circuit with less Area and since we have designed Adder using Carry look ahead approach by default we will achieve high speed and coming to the another important design constraint that is power by default STATIC CMOS logic, power consumption will be less.

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