INTERNATIONAL JOURNAL OF RECENT TRENDS IN ENGINEERING & RESEARCH
Impact Factor 4.101 ISSN -2455-1457
RECENT ADVANCES IN ELECTRONICS & COMMUNICATION ENGINEERING (RAECE-2K17)

DESIGN OF ADVANCED THERMAL SENSORS WHICH USES LOW POWER CONSUMPTION

J.H.N Harshini Pranitha
ECE Department
Nalla Narasimha Reddy
EducationalSociety's
Group of Institutions

D.Siri Deepika
ECE Department
Nalla Narasimha Reddy
EducationalSociety's
Group of Institutions

B.Sahithi
ECE Department
Nalla Narasimha Reddy
EducationalSociety's
Group of Institutions

Abstract: Thermal sensors (TS) are essential for achieving optimized performance and reliability in the era of nanoscale microprocessor and system on chip (SoC). Compiling with the low-power and small die area of the mobile computing, the presented TS supports a wide range of sampling frequencies with an optimized power envelope. The TS supports up to 45 K samples/s, low average power consumption, as low as 20 µW, and small core Si area of 0.013 mm^2. Advanced circuit techniques are used in order to overcome process variability, ensuring inaccuracy lower than ±2 °C without any calibration. All this makes the presented thermal sensor a cost-effective, low-power solution for 22 nm nanoscale digital process technology.**Keywords:** thermal sensor; sigma-delta Analog to Digital Converter (ADC); low-power; untrimmed temperature sensor; nanoscale digital process

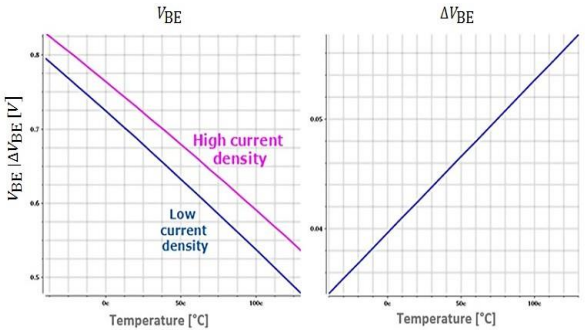
Introduction

Integrated thermal sensor (TS) circuits have become key elements in high performance ystems, especially in processors and system on chip (SoC). Such applications require a relatively high precision thermal sensor (typically ±3 °C in a wide temperature range), in order to achieve high reliability and performance [1,2]. The conventional method of thermal sensing is based on diode connected Bipolar Junction Transistor (BJT) voltage temperature dependence [2–7]. A base-emitter voltage equation of BJT transistor is :

$$V_{BE} = \frac{nkT}{q} Ln(\frac{I}{I_0}) \quad (1)$$

where n is the ideality factor of the diode, k is Boltzmann's constant, T is the absolute temperature, q is the electron charge, I_0 is the diode's saturation current and I is the current through the diode. This voltage is inversely proportional to the temperature, because of the strong temperature dependence of the saturation current I_0. Several motivations drove and guided the design of the temperature sensor presented in this paper:(a) to provide the best possible accuracy, as accurate temperature sensing extends performance of SoCs; (b) to utilize advanced circuit techniques to overcome process variance effects and, thus, to get a robust and accurate TS.

Figure 1. Operation principle of thermal sensor



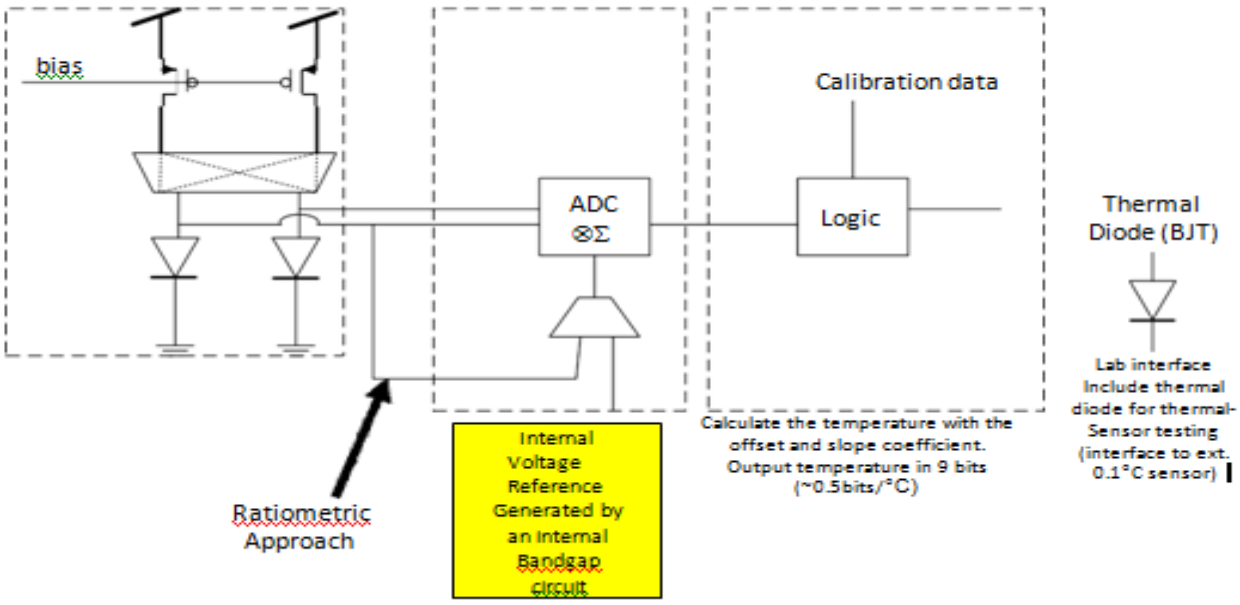
(CD—current density; a—temperature coefficient of ΔV_{BE}).

1. 22 nm Sigma-Delta Based Thermal Sensor Architecture

$$\Delta V_{BE} = (\frac{kT}{q})\ln(\frac{\text{highCD}}{\text{lowCD}}) \quad Sensitivity(a) = 138\frac{\mu V}{^{\circ}C}$$
$$\Delta V_{BE} = aT \quad for \text{ current density ratio of 5}$$

Better linearity is achieved using the Analog to Digital Converter (ADC) based thermal sensor [3,4]. The thermal sensor presented here was fabricated in the 22 nm process. The architecture includes an advanced sense stage combined with circuits that deal with process variations (chopping and dynamic element matching). A synthesized block implements the sigma-delta decimation filters and provides a digital readout of the relative operating temperature as well as temperature alerts. This sigma-delta ADC based TS can be operated in two modes: Reference-based (Vref) and Ratiometric-based. A thermal diode was also included within the TS for junction temperature sensing by a ±1 °C sensor, as part of the calibration process. The TS has two main power modes: high sampling rate and power saving.

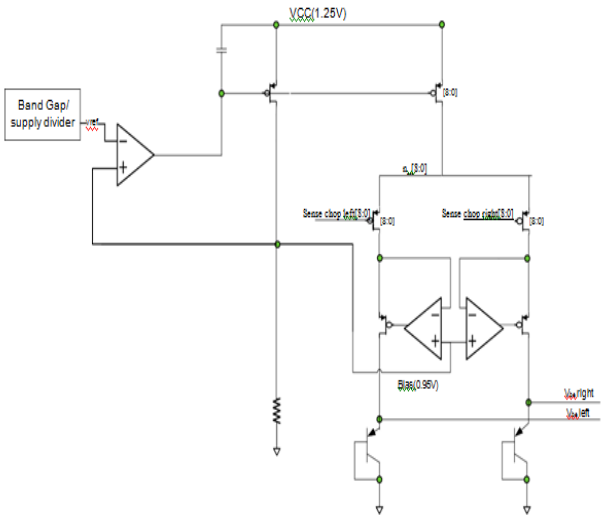
Figure 2. High level diagram of the Thermal Sensor.



2. The Sense Stage

The sense stage diagram, presented in Figure 3, converts the junction temperature to a Proportional to Absolute Temperature (PTAT) voltage. It includes a matched pair of diodes and current mirrors with controlled current ratios (of 3.5, 4, 5, 6, 7, and 8).

Figure 3. Sense stage block diagram.

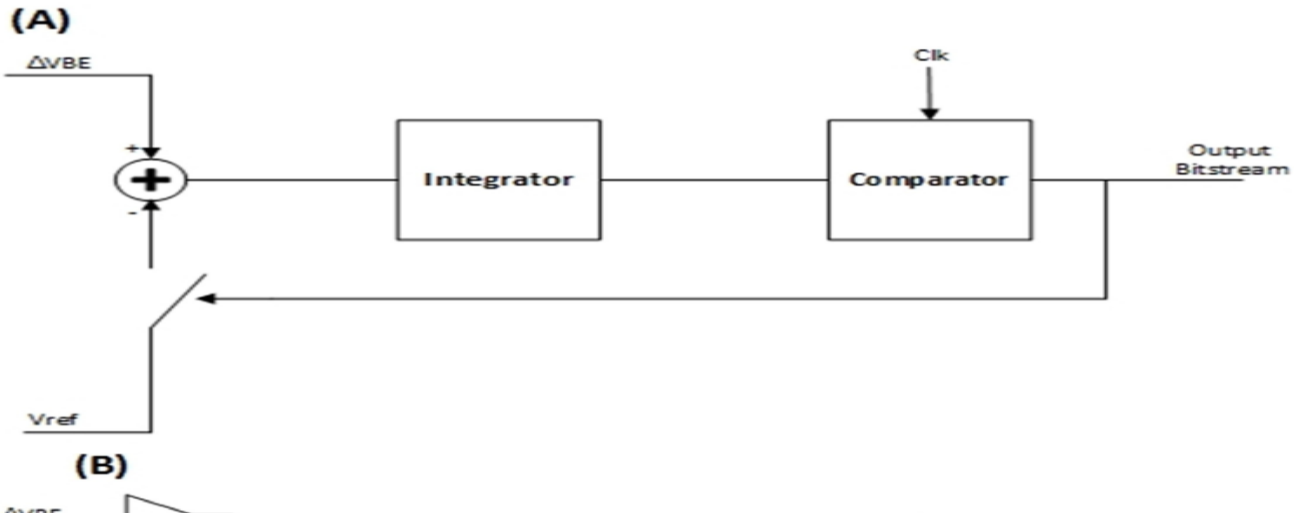


Chopping is also used by the sense circuit in order to overcome diode mismatches.From the circuit perspective, the sense stage is implemented with digital transistors on a relatively low power rail (1.25 V). The low threshold voltage of the digital transistors improves the circuits' headroom and improves the matching and Rout of the current mirrors and aids in achieving a good PSRR and an accurate TS in a small die area.

3. The Sigma-Delta Modulator

The sigma-delta modulator is a second order, one bit, switched-capacitor based design. Switched-capacitor circuits are frequently used for sigma-delta designs because they are fully compatible with digital CMOS processes. For low bandwidth applications, the over-sampling ratio (OSR) may be high enough so as not to limit the resolution of the ADC. A second order modulator is a preferred choice because it greatly reduces the stability problems of higher order modulators and decreases idle tone generation. The principles of the sigma-delta operation in the Vref-based and Ratiometric modes are presented in Figure 4. Charge balance is a fundamental property of any sigma-delta converter. This principle can be used to calculate the average signal transfer function of the modulator.

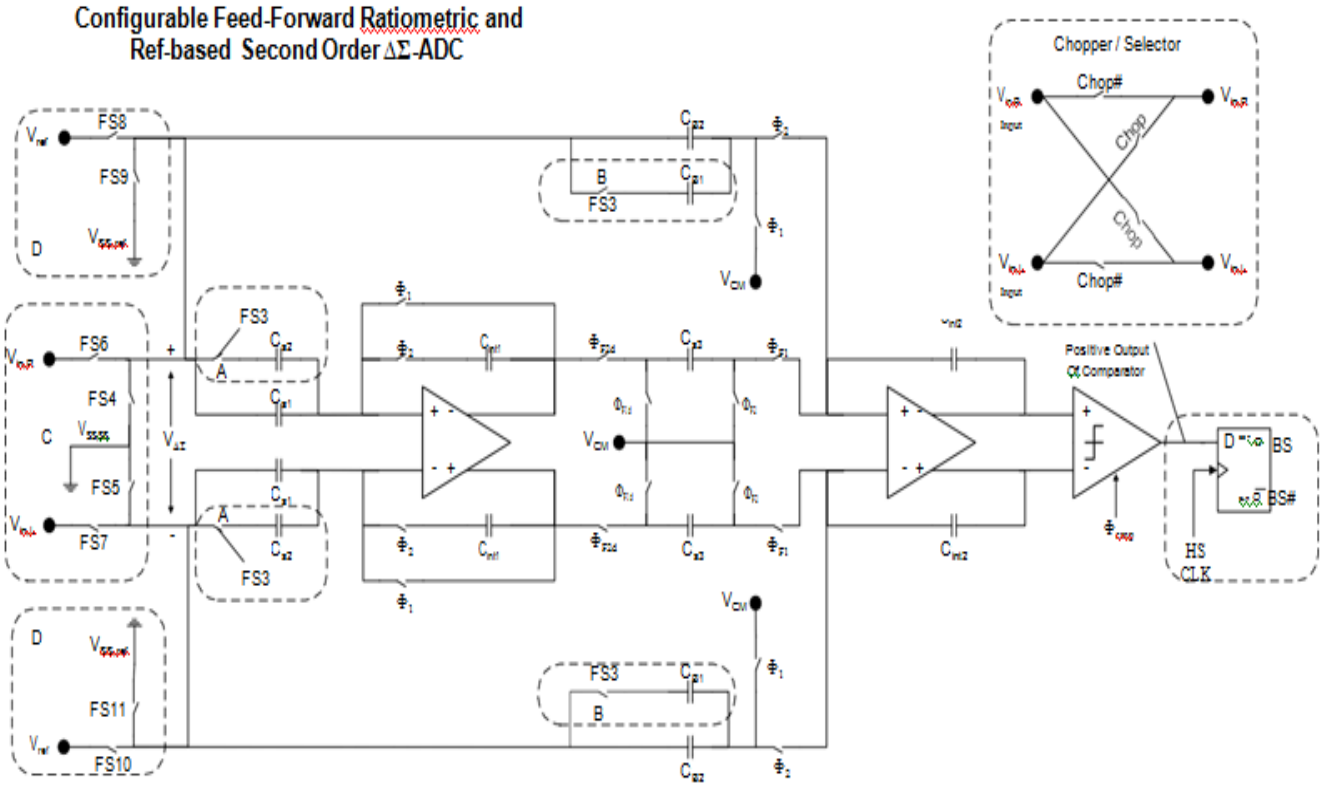
Figure 4. Sigma-delta Analog to Digital Converter (ADC) operation principle—(**A**) Vref mode; and (**B**) ratiometric mode.



Charge-balance mathematics are applied for demonstration to the reference-based sigma-delta, showing how the voltage ratio ($\Delta V_{BE}/V_{REF}$) is converted into an average duty ratio (or "1" density ratio) by the converter. The architecture of the sigma-delta converter is presented in Figure 5. The architecture is based on the converter presented by Pertijs and al [7]. Each amplifier constitutes an integrator, thus this circuit is a second order design .

.

Figure 5. Second order sigma-delta converter.



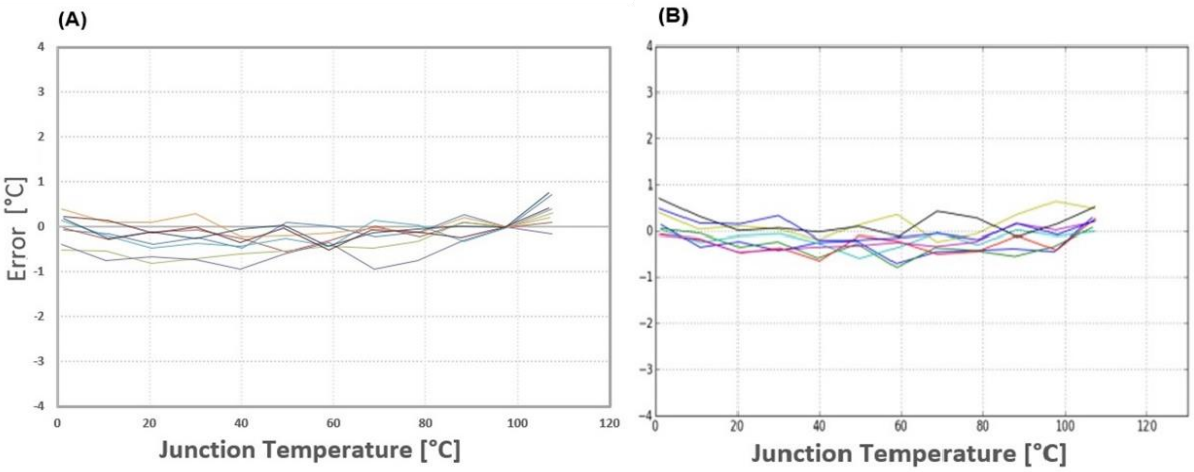
The second stage is a switch capacitor integrator. Feed-forward path stabilization causes low swing at the opamps'outputs so less distortion is expected. No DC component above CM voltage exists at the first integrator output.However, the feed-forward method makes the transfer function depend on capacitors' mismatch.

4. Results

The suggested SD-ADC based thermal sensor was implemented in a 22 nm process and was verified in two generations of test chips on typical and skew material. The evaluation boards included an adapter for a thermal head, which forces a specific temperature and an external component for checking the internal thermal diode for measuring the junctional temperature. Extracting the temperature inaccuracy of each chip was done in Ratiometric mode at a temperature range of 0–110 °C.

Figure 7A depicts the temperature reading errors of typical dies after one temperature calibration at 100 °C in Ratiometric mode with supply voltage of 1.25 V. The error for a wide range of temperature is smaller than ±1 °C. The results of the same chips only untrimmed (non-calibrated) demonstrates an inaccuracy of smaller than ±1 °C (Figure 7B). Note that these results include the error induced by the measuring procedure done by the thermal diode.

Figure 7. Temperature error *versus* junction temperature of different typical chips: (A) calibrated in one temperature and; (**B**) untrimmed.



The TS power consumption from the analog supply voltage (1.25 V) appears in Table 1. In the power saving mode in which the sampling rate is low (10–100 Sps), the power consumption is significantly reduced from ~1 mW in high sampling rate mode down to 18 µW.

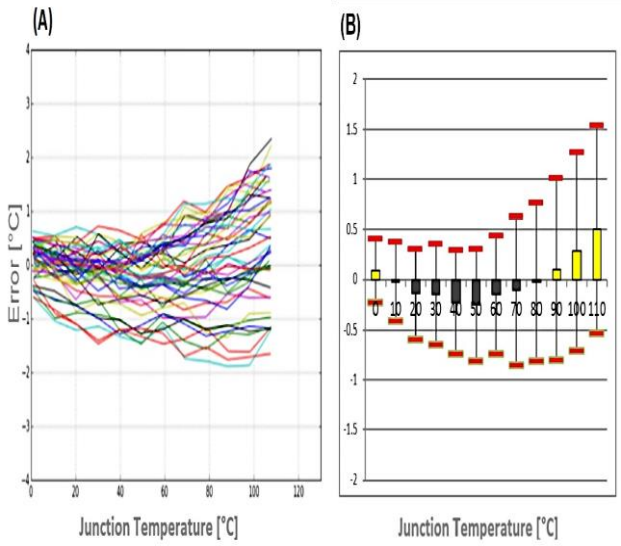
Table 1. Thermal Sensor power consumption for different sampling rates. "Typical" are the average numbers for typical die where "fast" results represent the absolute highest consumption measured for "fast" skew SI.

Power mode	Corner/Skew	Temp (C°)	Analog supply (V)	Analog current consumption (µA)	Analog power consumption (µW)
Power saving mode (10 Sps)	Typical	60	1.25	14	18
Power saving mode (10 Sps)	Fast	110	1.31	15	20
Power saving mode (100 Sps)	Typical	60	1.25	52	65
Power saving mode (100 Sps)	Fast	110	1.31	60	79
High sampling rate	Typical	60	1.25	780	975
High sampling rate	Fast	110	1.31	920	1205

Finally, the untrimmed inaccuracy, without using any calibration, is quite low (Figure 8) paving the way for using this TS without calibration for most SoC products. The error for 29 devices is ±2 °C in Ratiometric mode (Figure 9A). The average temperature error is <0.5 °C and the resolution is ±0.25 °C without any averaging of reading samples. The one sigma error is less than 1 °C (Figure 9B) and the three sigma error is less than ± 3 °C. Such inaccuracy is close to the results achieved by a practical calibration process such as using thermal diode. It means that calibration is unnecessary.

Figure 8. Untrimmed inaccuracy of thermal sensors in Ratiometric mode. (**A**) Temperature error *versus* junction temperature without calibration for 29 devices; (**B**) Statistics of errors presented in A. The yellow rectangle indicates the average error in a specific temperature and the error bar indicates the

standard deviation (1σ) of the error.



5. Summary

In this paper we presented a precise low power integrated thermal sensor. The architecture uses advanced features such as dynamic element matching, precise regulated cascode current mirror, chopping, and correlated double sampling to overcome accuracy and matching issues. Silicon validation performed demonstrates immunity to process variation and an error <±1.8 °C for a range of 0–110 °C with a single temperature calibration. Some of the configurability options were demonstrated, showing reference-based and Ratiometric operation. In the Ratiometric mode, a reference may not be needed as it is extracted by the ADC from the sense stage itself. Many additional configuration options, such as remote diode interfaces, signal path gain control, diode current ratio control and digital post processing options make this architecture a fertile testing ground for the exploration of temperature sensing techniques. The untrimmed inaccuracy of the thermal sensor is less than ±3 °C (3σ) across the entire range. Reducing the calibration process will significantly reduce the tester cost for SoC products. Over all, the silicon results show a unique ability to trade between high sampling rates and low power consumption up to 18 μW while retaining high accuracy without calibration in a small die area.

References

1. JEDEC Standard. *FBDIMM: Advanced Memory Buffer (AMB)*; JESD82–20; EDEC Solid State Technology ssociation: rlington, VA, USA, 2007.
2. Shor, J.S.; Luria, K. Miniaturized BJT-Based Thermal Sensor for icroprocessors in 32- and 22-nm Technologies. *IEEE J. Solid-State Circuits* **2013**, *48*, 2860–2867.
3. Sebastiano, F.; Breems, L.; Makinwa, K.A.A.; Drago, S.; Leenaerts, D.M.W.; Nauta, B. A 1.2-V 10-μW NPN-based temperature sensor in 65-nm CMOS with an inaccuracy of 0.2 °C (3σ) from 70 °C to 125 °C. *IEEE J. Solid-State Circuits* **2010**, *45*, 312–313.
4. Souri, K.; Chae, Y.; Makinwa, K.A.A. A CMOS temperature sensor with a voltage-calibrated inaccuracy of ±0.15 °C (3σ) from 55 °C to 125 °C. *IEEE J. Solid-State Circuits* **2013**, *48*, 292–301.
5. Lakdawala, H.; Li, Y.W.; ychowdhury, A.; Taylor, G.; Soumyanath, K. A 1.05 V 1.6 mW 0.45 °C 3σ-resolution ΔΣ-based temperature sensor with parasitic-resistance compensation in 32 nm CMOS. *IEEE J. Solid-State Circuits* **2009**, *44*, 340–341.
6. Pertijs, M.A.; Makinwa, K.A.A.; Huijsing, J. A CMOS smart temperature sensor with a 3 sigma inaccuracy of 0.1 C from 55 C to 125 C. *IEEE J. Solid-State Circuits* **2005**, *40*, 2805–2815.

7. Pertijs, M.A.; Niederkorn, A.; Ma, X.; McKillop, B.; Bakker, A.; Huijsing, J.H. A CMOS smart temperature sensor with a 3 sigma inaccuracy of 0.5 °C from 50 °C to 120 °C. *IEEE J. Solid-State Circuits* **2005**, *40*, 454–461.
8. Wang, G.; Meijer, G.C.M. The temperature characteristics of bipolar transistors fabricated in CMOS technology. *Sens. Actuators A* **2000**, *87*, 81–89.
9. Duarte, D.E.; Geannopoulos, G.; Mughal, U.; Wong, K.L.; Taylor, G. Temperature Sensor Design in a High Volume Manufacturing 65 nm CMOS Digital Process. In Proceedings of the IEEE 2007 Custom Integrated Circuits Conference, San Jose, CA, USA, 16–19 September 2007.

