



# Design of Low Power and High Speed 4-Bit Ripple Carry Adder Using area efficient full adder cell in 180nm CMOS Process Technology

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**Abstract**—Adders are basic components of digital design and necessary part of any digital signal Processing(DSP) architecture and microprocessors. In this paper design of a 4-bit ripple carry adder is proposed using a novel 18-transistor CMOS transmission gate full adder cell. The main objective is to reduce area by decreasing the transistor count compared with the ripple carry adder using conventional full adder. The design is implemented using Cadence Virtuoso schematic editor and simulated using Cadence Virtuoso analog design environment at 180nm CMOS process technology. The simulation results of the ripple carry adder using the proposed full adder cell are compared with ripple carry adder using conventional full adder cell in terms of transistor count, delay and power. The number of transistors is reduced from 28 in conventional full adder to 18 in the proposed transmission gate full adder. As a result the proposed 4-bit ripple carry adder with 72 transistors is efficient in terms of area.

**Index Terms**—Cadence, delay, area efficient, full adder, ripple carry adder, schematic, transmission gate and XOR gate.

## I. INTRODUCTION

Most of the VLSI applications, such as digital signal processing, image and video processing and microprocessors, extensively use arithmetic operations. Addition, subtraction, multiplication and multiply and accumulate (MAC) are examples of the most commonly used operations. The 1-bit full-adder cell is the building block of all these modules. Thus, enhancing its performance is critical for enhancing the overall module performance. The most important performance parameters for future VLSI systems are speed and power consumption. In this paper we present a novel 1-bit full adder cell which offers faster operation and consumes less area and power than standard implementations of the full adder cell.

With the popularity of portable systems as well as fast growth of power density in integrated circuits, power dissipation becomes main design objectives equal to high performance of the system. For the VLSI designers, designing power efficient adders for digital system has become main goal. Generally ripple carry adders are used among all types of adders because of its compact design but it is the slowest adder.

Several ripple carry adders have been proposed using different full adder cells targeting on design accents such as power, delay and area. Among those designs with less transistor count using transmission gate logic have been widely used to reduce area. The proposed ripple carry adder is implemented using Cadence EDA tool [2]. The tool provides sophisticated features such as Cadence Virtuoso Schematic Editor which provides sophisticated capabilities which speed and ease the design, Cadence

performance of the design and Cadence Virtuoso Layout Suite that speeds up the physical layout of the design.

In this paper, we propose a design of ripple carry adder using full adder cell with 18 transistors. The paper is organized as follows: in section II, previous work is reviewed. Subsequently, in section III, the proposed design of ripple carry adder is presented. In section IV, the schematic and layout of the adders are presented. In section V, the simulation results are given and discussed. The comparison and evaluation for proposed and conventional designs are carried out. Finally a conclusion will be made in the last section.

## II. EXISTING SYSTEM

Adding two single-bit binary values with the inclusion of a carry input produces two outputs, a sum and a carry; this circuit is called a full adder. The relation between the inputs A, B, Cin and the outputs Sum and Cout are expressed as:

$$\text{Sum} = A \oplus B \oplus C_{in}$$

$$\text{Cout} = AB + BC + CA$$

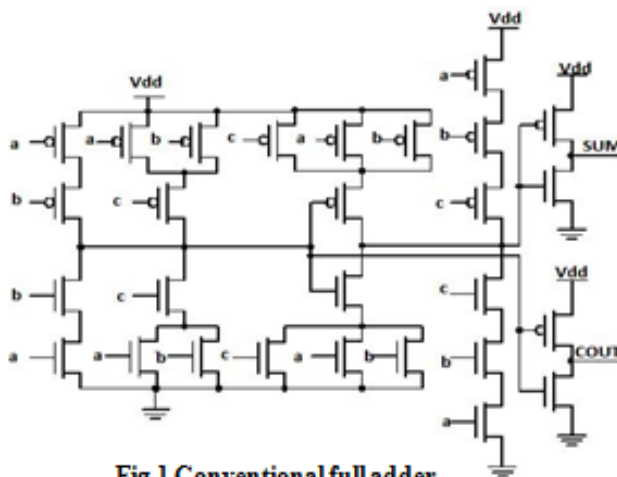


Fig.1 Conventional full adder

The truth table of full adder is shown below.

Inputs			Outputs	
A	B	Cin	Sum	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Different logic styles can be investigated from different points of view. Evidently, they tend to favor one performance aspect at the expense of others. In other words, it is different design constraints imposed by the application that each logic style has its place in the cell library development. Even a selected style appropriate for a specific function may not be suitable for another one. For example, static approach presents robustness against noise effects, so automatically provides a reliable operation. The issue of ease of design is not always attained easily. The CMOS design style is not area efficient for complex gates with large fan-ins. Thus, care must be taken when a static logic style is selected to realize a logic function.

The conventional full adder shown in Fig.1 is a complementary CMOS (C-CMOS) full adder with 28 transistors [4]. It is a combination of PMOS pull up transistors and NMOS pull down transistors [5]. It is well known for its robustness and scalability at low supply voltages. The complementary CMOS logic circuit has the advantages of layout regularity and stability at low voltage due to the complementary transistor pairs and smaller number of interconnecting wires. But its power consumption and transistor count are relatively high for low power arithmetic circuits. In this full adder, interdependence between signals generation (SUM signal relies on the generation of COUT signal) causes the problem of delay imbalance.

rtuoso Visualization and Analysis which efficiently analyzes the

Ripple carry adder is built using multiple full adders such as the above discussed conventional full adder. In ripple carry adder each carry bit from a full adder "ripples" to the next full adder. The simple implementation of 4-bit ripple carry adder is shown below.  $C_0$  is the input carry,  $x_0$  through  $x_3$  and  $y_0$  through  $y_3$  represents two 4-bit input binary numbers.

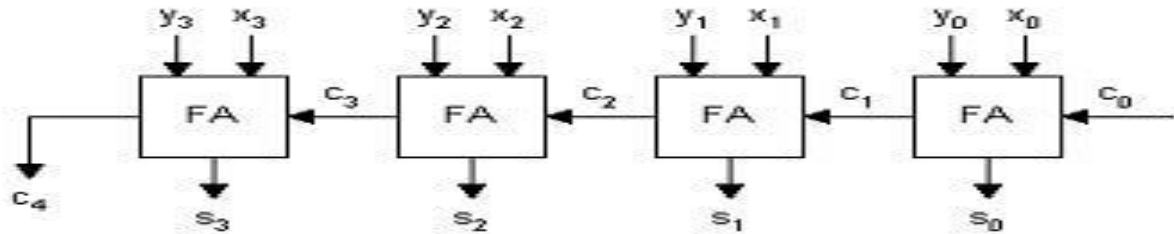


Fig.2 4-bit ripple carry adder

### III. PROPOSED RIPPLE CARRY ADDER

The proposed ripple carry adder is designed using a full adder cell with 18-transistors based on transmission gate [7]. It uses a novel exclusive-or (XOR) gate. The schematic for this XOR gate is shown in Fig.3.

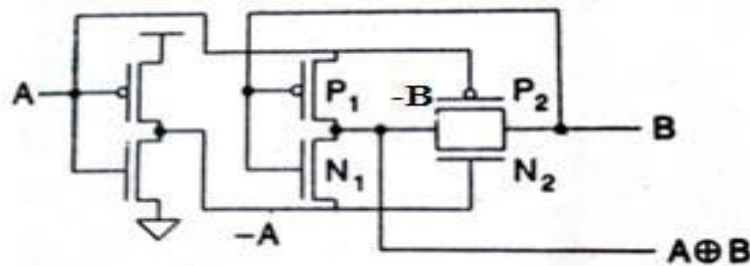
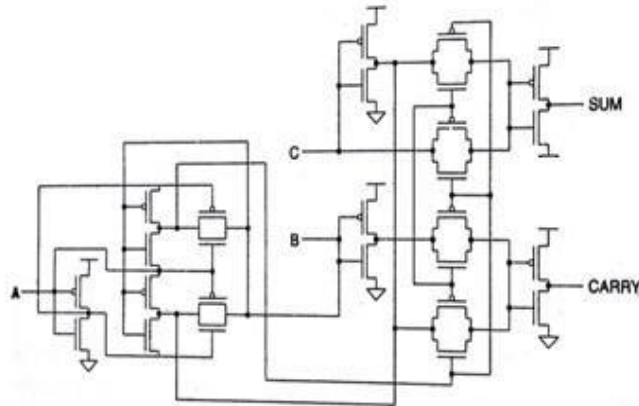


Fig.3 Transmission gate XOR

As a point to note, switch-level simulators have problems with this gate. The operation of the gate is explained as follows:

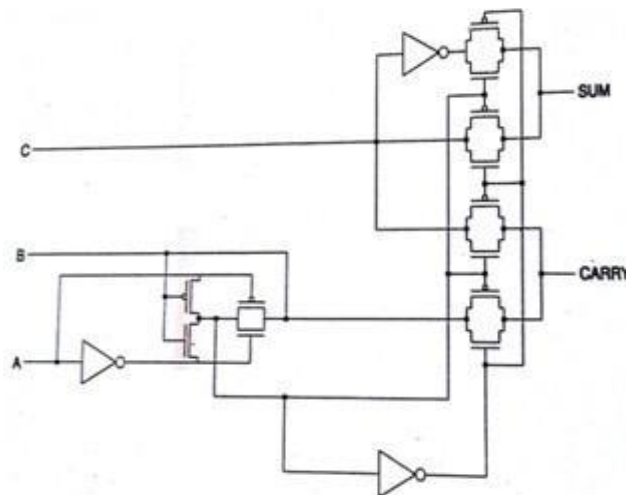
1. When signal  $A$  is high,  $-A$  is low. Transistor pair  $P_1$  and  $N_1$  thus acts as inverter, with  $-B$  appearing at the output. The transmission gate formed by transistor pair  $P_2$  and  $N_2$  is open.
2. When signal  $A$  is low,  $-A$  is high. The transmission gate formed by transistor pair  $P_2$  and  $N_2$  is now closed, passing  $B$  to the output. The inverter formed by transistor pair  $P_1$  and  $N_1$  is partially disabled (level reduced  $B$  passed to the output by  $P_1, N_1$ ).

Thus this transistor configuration forms a 6-transistor XOR gate. By reversing the connections of A and  $\bar{A}$ , an exclusive-nor (XNOR) gate is constructed [7].



**Fig.4 Transmission gate full adder**

By using four transmission gates, four inverters and two XOR gates, an adder may be constructed according to Fig.4.  $A \text{ xor } B$  and the complement are formed using the transmission gate XOR gate shown in Fig.3. The SUM ( $A \text{ xor } B \text{ xor } C_{in}$ ) is formed by a multiplexer controlled by  $A \text{ xor } B$  (and complement). Examining the adder truth table reveals that  $C_{OUT} = C$  when  $A \text{ xor } B$  is true. When  $A \text{ xor } B$  is false,  $C_{OUT} = A$  (or  $B$ ). This adder has 26 transistors and equal SUM and COUT delay times.



**Fig.5 Optimized transmission gate full adder**

The number of transistors may be reduced if speed is not the ultimate goal. Two transistors may be eliminated by using an inverter on the output of the XOR gate [7]. In addition with some optimization, the output buffers may be eliminated, as shown in Fig.5.

Thus the proposed ripple carry adder is implemented using optimized transmission gate full adder which is efficient in terms of area.

IV. SCHEMATIC AND LAYOUT

All the above discussed adders are implemented in Cadence EDA tool. The transistor level diagram is implemented using Cadence Virtuoso schematic editor. The optimized layout is built using Cadence Virtuoso Layout Suite.

A. Schematic

The schematic diagram of the conventional full adder and the proposed transmission gate full adder cells are built using PMOS and NMOS transistors with the following specifications.

The schematic diagrams of the conventional complementary CMOS (C-CMOS) full adder using 28 transistors and ripple carry adder using it are as shown in Fig.6 .

	:
Length	180nm
Total width	: 2 $\mu$ m
Finger width	: 2 $\mu$ m
Fingers	: 1
	:
S/D metal	400nm
	:
Threshold	800nm

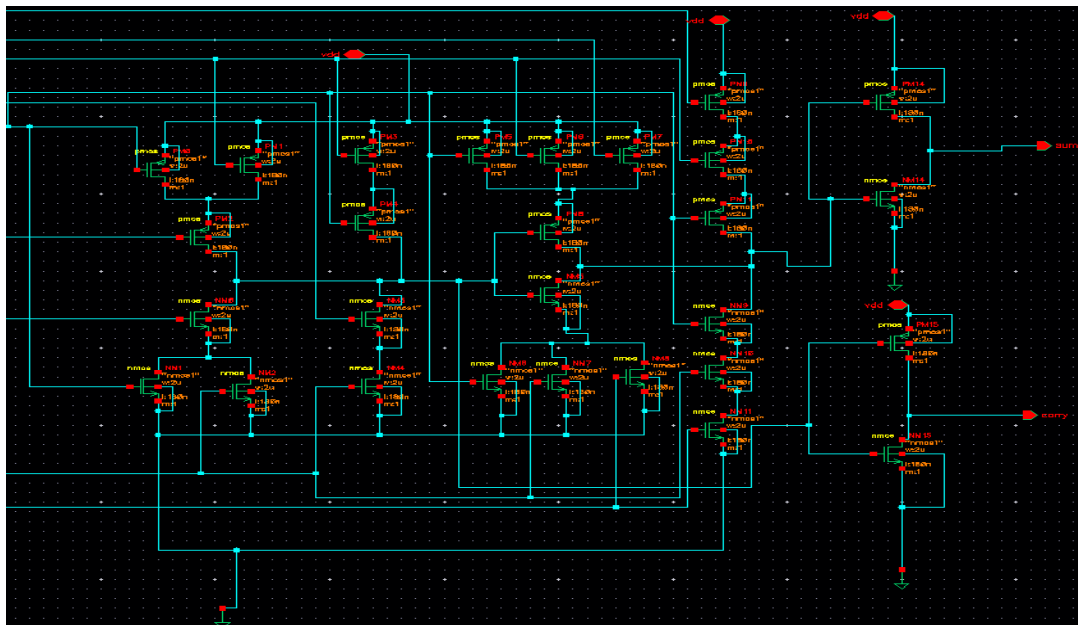


Fig.6 Schematic of conventional full adder

The schematic diagrams of the proposed optimized transmission gate full adder using 18 transistors and ripple carry adder using it are as shown in Fig.7 and Fig.8 respectively.

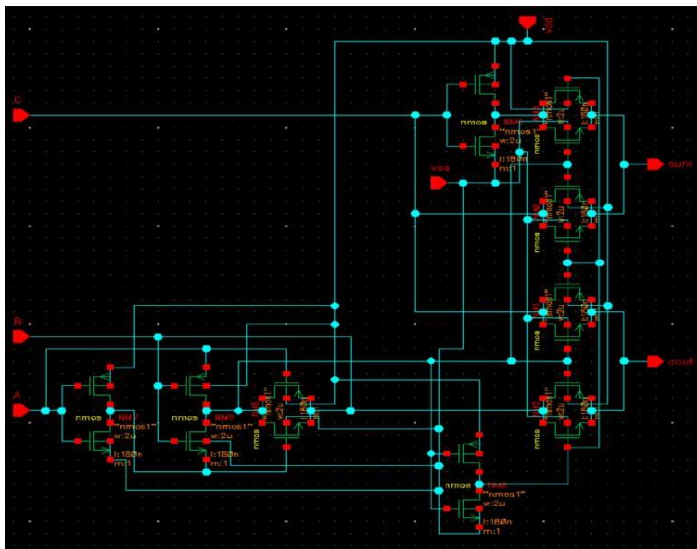


Fig.7 Schematic of optimized TG full adder

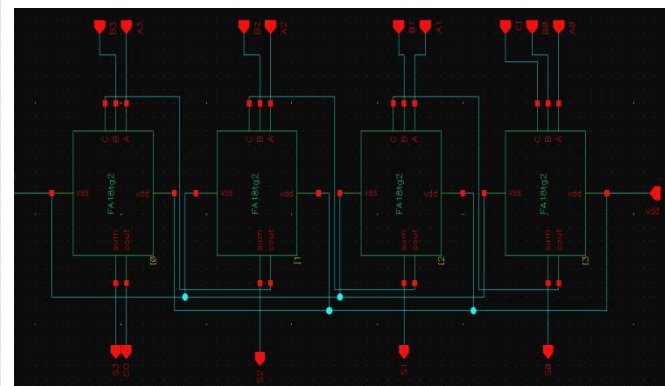


Fig.8 Schematic of ripple carry adder using optimized TG full adder

### V. SIMULATION AND RESULTS

The simulation results of the conventional full adder and ripple carry adder using it are as shown below in Fig.09 and Fig.10 respectively. The ripple carry adders using conventional and proposed full adder are simulated for the following inputs.

A3 A2 A1 A0 – 0 1 0 1  
 B3 B2 B1 B0 – 0 1 1 0  
 Cin – 1

S3 S2 S1 S0 – 1 1 0 0  
 Cout – 0

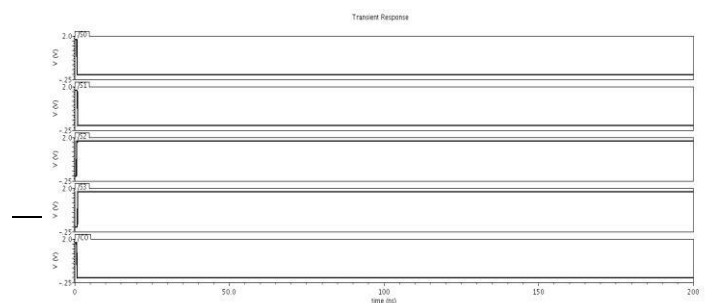
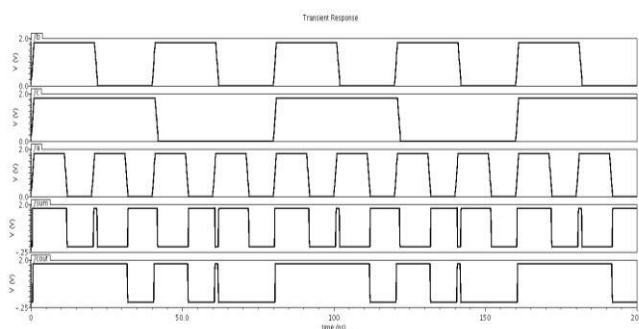


Fig.09 Simulation of conventional full adder

Fig.10 Simulation of ripple carry adder using conventional full adder

The simulation results of optimized transmission gate full adder with 18 transistors and ripple carry adder using it are as shown below in Fig.11 and Fig. 12 respectively.

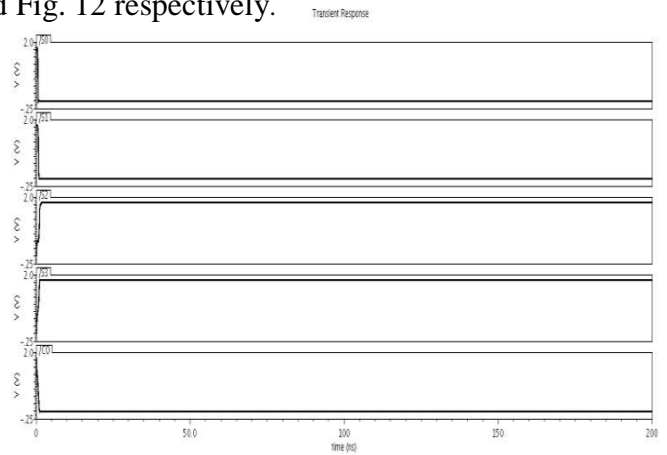
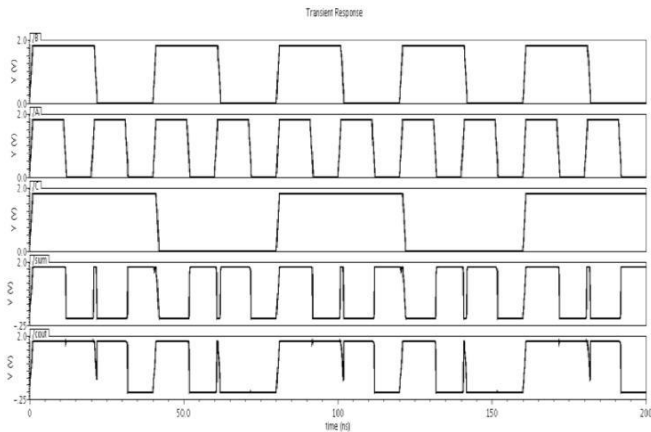


Fig.11 Simulation of 18T optimized TG full adder

Fig.12 Simulation of ripple carry adder using 18T optimized TG full adder

The comparison of transistor count, delay and power between all the above discussed full adders is done below.

Table 2. Transistor count, delay and power comparison between full adders

Full adder	Transistor count	Delay	Power
Conventional full adder	28	324.0 ps	18.5 $\mu$ W
Optimized TG full adder	18	225.5 ps	22.01 $\mu$ W
Ripple carry adder using conventional full adder	112	350.5 ps	4.324 $\mu$ W
Ripple carry adder using optimized TG	72	254.4 ps	3.522 $\mu$ W

full adder			
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## VI. CONCLUSION

In this paper two different ripple carry adders have been implemented, simulated, analyzed and compared. A novel full adder designed using 18 transmission gate is presented in this paper that targets low transistor count and area. The characteristics of the adder circuit are compared against conventional complementary CMOS full adder based on the transistor count and delay. The optimized layout is drawn for the proposed full adder cell and the ripple carry adder in Cadence tool using sea of gate arrays concept. Thus we have implemented a ripple carry adder which is optimized in terms of transistor count and area and is more efficient than the ripple carry adder using conventional complementary CMOS full adder.

## REFERENCE

- [1] Ahmed M. Shams and Magdy A. Bayoumi, —A Novel High-Performance CMOS 1-Bit Full-Adder Cell|| IEEE transactions on circuits and systems—II: Analog and digital signal processing, Vol. 47, NO. 5, MAY 2000.
- [2] Cadence Analog and Mixed signal labs, revision 1.0, IC613, Assura 32, incisive unified simulator 82, Cadence design systems, Bangalore.
- [3]Dan Wang, Maofeng Yang, Wu Cheng XUguang Guan, Zhangming Zhu, Yintang Yang — Novel Low power Full Adder Cells in 180nm CMOS Technology||, 4th IEEE conference on Industrial Electronics and Applications, pp. 430-433,2009.
- [4] Karthik Reddy. G, —Low Power-Area Designs Of 1 BitFull Adder in Cadence Virtuoso Platform||, International Journal of VLSI design & Communication Systems (VLSICS) Vol.4, No.4, August 2013.
- [5]Kavita Khare, Krishna Dayal Shukla, —Design A 1Bit Low Power Full Adder Using Cadence Tool||, MANIT/ Electronics & Communication, Bhopal, India
- [6] M.Geetha Priya, K.Baskaran, —Low Power Full Adder With Reduced Transistor Count||, International Journal of Engineering Trends and Technology (IJETT) – Volume 4 Issue 5- May 2013.
- [7] Neil H. E. Weste, Kamran Eshranhian, —Principles of CMOS VLSI Design,|| A systems Perspective, 2<sup>nd</sup> edition.



