

High Speed Level Shifters for Low Power Applications with Reduced Size

Priyanka Boshetty

Department of Electronics and
Communications Engg.
NNRG College of Engineering,
Hyderabad, India

Umadevi Gurram

Department of Electronics and
Communications Engg.
NNRG College of Engineering,
Hyderabad, India

Srinivas Reddy Panati

Department of Electronics and
Communications Engg.
NNRG College of Engineering,
Hyderabad, India

Abstract — In this paper a high speed level shifter is proposed for low power applications. This circuit is a power efficient level shifter that converts low level input voltages to high level voltages as per the design requirement. The efficiency of pull up and pull down transistors are improved in the proposed method and the circuit was tested by using 180 nm CMOS technology. A unit buffer and inverter circuit was introduced to the load circuits and input buffers to have fair comparison between different structures. The overall power consumption in the proposed circuit was reduced to a minimum level by reducing the number of transistors to build a level shifter.

Keywords—Level Shifter, Low Power, Source Follower, CMOS Technology.

I. INTRODUCTION

In day to day life, there is a need of increase in handheld devices like mobile phones, cameras, speakers etc. With the increase in these portable devices, low power consumption has become an important issue in integrated circuits. The heat dissipation caused by enormous power consumption creates a problem that badly effect the reliability, efficiency and cost of the system design. In order to develop techniques for minimizing power dissipation, it is essential to identify various sources of power dissipation and different parameters involved in each of them. The total power for a VLSI circuit consists of dynamic power and static power. In (SoC) design, different components are fabricated on a single chip and needs different voltages to obtain optimum performance. In modern VLSI system circuits, the design of level shifters using multiple supply voltages has been widely used. Multi Supply Voltage Domain (MSVD) technique is an effective method to reduce dynamic, static and leakage Power in modern system-on-chips. Dynamic power results due to switching of load capacitance between two different voltage logic levels. Static power is caused due to short circuit paths between the supply voltage and ground. Leakage power results in leakage currents that arise from substrate injection and sub-threshold [7]. Level shifters are used as an interface between different voltage domains. In multi supply voltage system design, a level shifter is used to convert from voltage level to another voltage level. Conventional level shifter is capable of handling low voltage input and shifts any voltage level to a desired voltage level [1].

A low voltage signal may not have threshold value more than that of high voltage signal. Therefore, a level shifter is used to interface between two different voltage domains. A Conventional level shifter consists of a cross coupled PMOS and NMOS driven by an input signal. When low voltage circuit drives high voltage circuit the PMOS of high voltage domain does not turn off completely by low voltage circuit. As a result, it leads to increase in leakage currents and power consumption. Hence level shifters are used to reduce unwanted power consumption.



Fig. 1. Basic block diagram of level Shifter

A. Level Shifter

Due to advancement in VLSI technology, leads to complex circuits resulting in increase in functionality and power dissipation. Energy Efficiency is a primary concern in modern CMOS circuits. The major sources of power dissipation are static and dynamic power. Static power is mainly due to leakage currents, whereas dynamic power is due to supply voltages and charging and discharging of load capacitance [5]. The dynamic energy is directly proportional to supply voltage. Low supply voltage results in decreasing in dynamic power quadratically [6]. That is, higher the supply voltage higher the energy consumption. In order to reduce the dynamic power consumption without degrading the performance of the circuit level shifters are used. For analog and mixed signal circuits level shifter plays a crucial role. The low power level shifter circuit consists of three stages input stage, level shifter or level converter, output stage. The main objective of each level shifter is to reduce power dissipation, reduce chip size, area and to decrease the cost of integrated circuits.

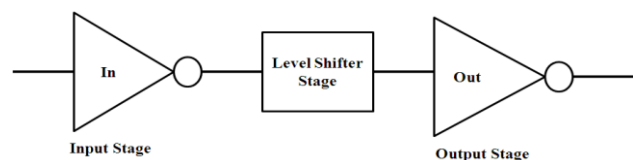


Fig. 2. Level Shifter circuit

There are two types of level shifters:

- Single supply level shifter (SSLS)
- Dual supply level shifter (DSLS)

The single supply voltage level shifters suffer from high leakage currents. In a System DSLS provide bidirectional voltage translators with high speed. The dual supply voltage level shifters are suitable for mixed voltage systems which provide bidirectional level shifting in a wide range of supply voltages. Level shifters are the logic elements to be placed properly to ensure proper power domain crossing. By scaling down the size of MOS transistor, problems like high power density, high leakage currents, and parametric variations can be limited through the use of level shifters [6].

II. LITERATURE SURVEY

In the electronic world due to increased demands for the portable devices and low power electronic systems the demand for scaling down the transistors size is increasing with time. To design most of the CMOS devices using VLSI technology, the NMOS and PMOS sub circuits are being doped into the P+ regions labeling them as drain and source with a proper distance between them by inserting gate terminal to separate it by silicon dioxide (SiO₂) layer. Two regions of N+ are used to create a NMOS device using a lightly doped p Substrate. A lot of importance is given for the leakage powers in VLSI technology which in general tends to increase for any kind of errors at the time of designing [1]. There are baleful design concerns in the circuits designed using VLSI technology due to large applications are based on battery based devices such as personal computers, mobile phones, PDAs, etc. In a single, chip using nanometer technology contain millions of transistors and the heat dissipation due to each transistor consumes enormous power which impacts on the reliability and packaging cost of the overall design [2]. The research is being carried out at different levels to improve the power reduction techniques and to improve the low power design circuits [3]. Another method to solve the power consumption problem is by using the multi supply voltage domain techniques [4] where the voltage level depends on the time and requirement. To maximize the performance time critical domains are driven at high power supply voltages and for low power supply voltages non critical sections will drive to increase the power efficiency [2]. To reduce the power consumption when the transistors are in active modes adaptive voltage level at ground (AVLG) and adaptive voltage level supply (AVLS) are used [5].

There are various level shifters proposed by different authors in the recent times are listed here for a brief introduction of the recent research activities in this area. Lanuzza et al. proposed a level shifter using 90nm technology that converts 100mV signals to 1V signals [2]. The work carried out in this research guarantees robust voltage shifting with a fast response at a very low consumption of the energy. However, this circuit is with a drawback of 16.6 nS delay and 8.7 nW of static power dissipation. In a similar attempt Shapiro and Friedman proposed a power efficient level shifter using FinFET using 16 nm technologies for the near threshold circuits. This level shifter is capable of level shifting the voltages from 250 mV to 790 mV with a 42% shorter delay at a very low energy consumption of 45% and with low static power dissipation of 48% [4].

Later, Kumar et al. experimented to reduce the leakage power using stacking technique for designing a level shifter that is functioning with small leakage currents [5]. The authors in this work explained the reasons for the delay variations due to current driving capacity of different transistors which in real allow the design engineers to experience larger power consumptions. However, Moghaddam et al. reported the methods of scaling down of the transistor sized using complementary metal oxide semiconductors by using high lateral electric fields. But in such situations the short channel effects become very important [6]. The designing of low power, high gain and performance with fewer transistors in a chip have the impact on the cost of the overall circuit design. In this work the authors used back gate of planar double gate SOIFET was used to tune the threshold voltage of the devices. Similar experiment like Kumar et al. [5] to propose a low power voltage level shifter using AVLG and AVLS was carried out by Sharma et al. [7] to reduce the active power and leakage power at the level of nano scales. The results in this work could minimize the threshold leakage currents as compared to AVLG. AVLS was reported to be one of the best techniques to reduce the power consumption at low threshold voltages. To reduce the supply round and layout congestion within a chip Khan et al. proposed a multi-voltage system using 90 nm CMOS technology. This proposed level shifter can shift the voltages from 1.2 V to 2.5 V at a maximum operating frequency of 500 MHz. Later Srinivasulu et al. suggested a standard level shifter using differential cascade voltage switch (DCVS), which helped to enhance the performance characteristics such as speed, etc. of a circuit. Haga and Kale also suggested a programmable DC level shifter with very less threshold voltages using bulk driven MOSFET with a reverse biased voltage for shifting the input [10]. Various problems associated with single supply voltage level shifters was explained by Manohar et al. using bidirectional single supply voltages [11]. To overcome the problems related leakage current using short channels devices was suggested by Agarwal et al. using the concept of power gating and MTCMOS [12]. This circuit was best suited for the deep sub-micron based ASIC devices for low power applications for voltage conversions from low to high and high to low levels. A level shifter inserted in white space of the chip was proposed by Lin et al. to increase the wire length however it proved to be making power planning very difficult [13].

Full swing and floating type level shifter was proposed by Zheng et al. to operate at high speed due to high power consumption and larger layout area [14]. A simplified model of level shifter was proposed based on the mathematical analysis and it helped to improve the performance characteristics of the circuits. As a result design cost and chip area found to be minimized. A level shifter with preamplifier along with an error correction circuit and also an output latch stage was proposed by Matsuzka et al. proved to be dissipating large energy and have long transition time [15]. Since the circuit is based on a single transistor to help reducing the cost of the design.

III. METHODOLOGY

Designing a CMOS based source follower circuit is very difficult due to low values of transconductance is reported as compared to BJT. The importance for

transconductance is due to the impact on gain of an amplifier and in general it is less than 1. A source follower is applicable to use it as a voltage buffer and also as a level shifter. The DC values can be changed by changing the aspect ratio of the MOSFET and therefore it is very simple and flexible to use a source follower circuit as a level shifter.

In the following sections a detailed analysis of the level shifter is presented here for analyzing the circuit performance. Consider a source follower circuit as shown in Fig. 3 with a load R_s .

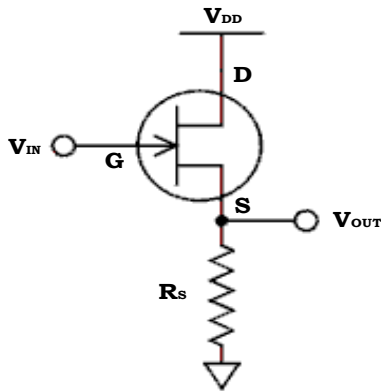


Fig. 3. Source follower circuit with load

The buffer used after the amplifier to drive the low impedance load and losses in signals can be ignored or negligible. The input for this circuit is applied at gate and output is taken at the source. Consider constant gate to source voltage and in such circumstances the output will be equal to input voltage along with added offset voltage as well.

The small signal analysis for the circuit shown in Fig. 3 is given below:

Applying KVL at input loop,

$$V_{in} = V_{gs} + V_{out} \tag{1}$$

here, $V_{gs} = V_{in} - V_{out}$

When output is open circuited, $i_o=0$ and applying KCL at output node gives

$$gmV_{gs} - g_{mb}V_{out} - \frac{V_{out}}{R_L} - \frac{V_{out}}{r_o} = 0 \tag{2}$$

Now substitute V_{gs} from Eq. (1) into Eq. (2) and rearranging

$$gm(V_{in} - V_{out}) - g_{mb}V_{out} - \frac{V_{out}}{R_L} - \frac{V_{out}}{r_o} = 0$$

$$gmV_{in} = gmV_{out} + g_{mb}V_{out} + \frac{V_{out}}{R_L} + \frac{V_{out}}{r_o} = 0$$

Now, V_{out}/V_{in} is

$$\frac{V_{out}}{V_{in}} = \frac{gm}{gm + g_{mb} + \frac{1}{R_L} + \frac{1}{r_o}}$$

$$\frac{V_{out}}{V_{in}} = \frac{gmr_o}{1 + (gm + g_{mb})r_o + \frac{r_o}{R_L}} \tag{3}$$

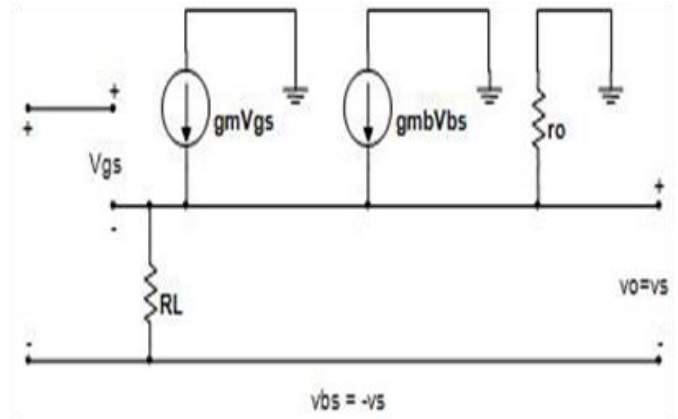


Fig. 4. Small signal analysis of source follower

If $R_L \rightarrow \infty$, then Eq. (3) is written as

$$\lim_{R_L \rightarrow \infty} \frac{V_{out}}{V_{in}} = \frac{gmr_o}{1 + (gm + g_{mb})r_o} \tag{4}$$

If r_o is finite, then the gain of small signal value is less than unity. Therefore consider $R_L \rightarrow \infty, r_o \rightarrow \infty$,

$$\lim_{\substack{R_L \rightarrow \infty \\ r_o \rightarrow \infty}} \frac{V_{out}}{V_{in}} = \frac{gm}{gm + g_{mb}} = \frac{1}{1 + \chi} \tag{5}$$

From Eq. (5) the voltage gain is less than unity as $\chi = g_{mb}/gm$ and its range is from 0.1 to 0.3, as a result it causes distortion in large signal changes in the output. This can be overcome by selecting a source follower fabricated in an isolated well. The output resistance of can be calculated by setting $V_{in}=0$ and $V_{gs}=V_{out}$, then i_o is

$$i_o = gmV_{out} + g_{mb}V_{out} + \frac{V_{out}}{R_L} + \frac{V_{out}}{r_o} \tag{6}$$

Then

$$R_o = \frac{V_{out}}{i_o} = \frac{1}{gm + g_{mb} + \frac{1}{R_L} + \frac{1}{r_o}} \tag{7}$$

These source followers can be used as buffers and level shifters. They are more flexible as level shifter because the dc value can be changed according to the aspect ratio W/L .

A. Proposed Super Source Follower Circuit

The output resistance of source follower is too high ($\frac{1}{gm + g_{mb}}$) to drive a resistive load. This can be reduced by increasing the aspect ratio and its dc bias current; as a result, area and power consumption will increase. To minimize the area and power consumption, we proposed a super source follower circuit which uses negative feedback to reduce output resistance.

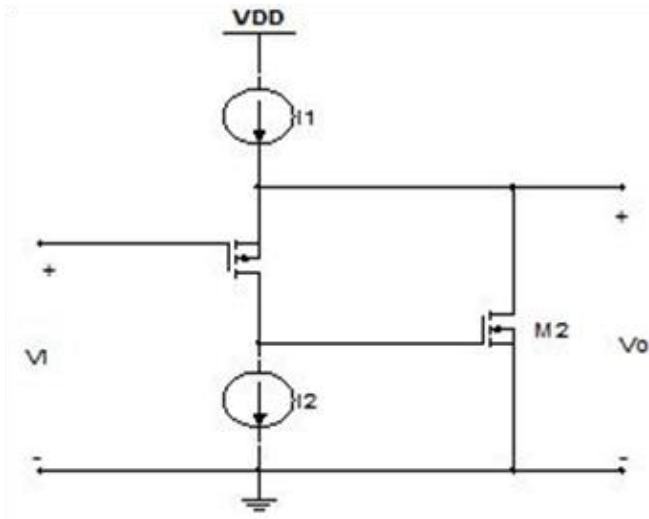


Fig. 5. Super source follower circuit

The above circuit can be analyzed as follows: when input voltage is constant the output voltages increases and drain current of M1 increases resulting in increased in gate source voltage of M2. The drain current of M2 increases, reducing the output resistance. For proper operation, the dc bias current of M2 is different between I_1 and I_2 hence we consider $I_1 > I_2$ through small signal analysis where I_1 and I_2 are replaced by internal resistances r_1 and r_2 respectively. To find the output resistance of super source follower set $V_{in}=0$. Apply KCL at output node, we get i_o as

$$i_o = \frac{V_2}{r_2} + g_{m2}V_2 + \frac{V_{out}}{r_1} + \frac{V_{out}}{r_{o2}} \quad (8)$$

Apply KCL at M1 with $V_{in}=0$,

$$\frac{V_2}{r_2} - g_{m1}V_{out} - g_{mb1}V_{out} + \frac{V_2 - V_{out}}{r_{o1}} = 0 \quad (9)$$

Substituting Eq. (9) in (8) and rearranging we get,

$$R_o = \frac{V_{out}}{i_o} = r_1 || r_{o2} || \left(\frac{r_{o1} + r_2}{1 + (g_{m1} + g_{mb1})r_{o1}(1 + g_{m2}r_2)} \right) \quad (10)$$

Assume I_1 and I_2 to be ideal sources, also $r_{o1} \rightarrow \infty$ and $(g_{m1} + g_{mb1})r_{o1} \gg 1$

$$R_o \cong \frac{1}{g_{m1} + g_{mb1}} \left(\frac{1}{g_{m2}r_{o1}} \right) \quad (11)$$

From Eq. (3.11) and (3.7), it can be seen that the output resistance of super source follower is reduced by factor of $g_{m2}r_{o1}$.

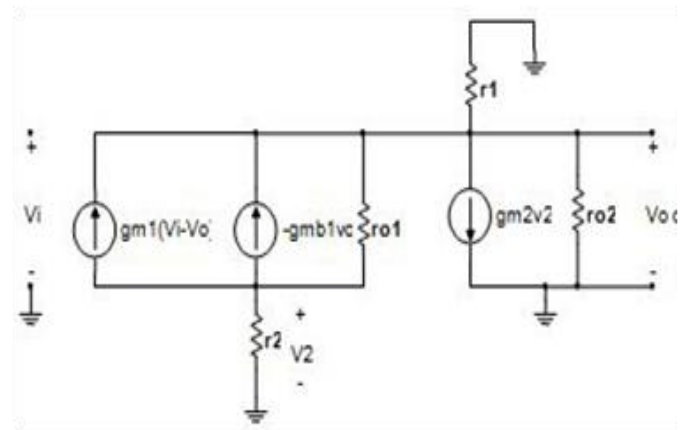


Fig. 6. Small signal analysis of super source follower

Applying KCL at output node gives

$$\frac{V_2}{r_2} + g_{m2}V_2 + \frac{V_{out}}{r_1} + \frac{V_{out}}{r_{o2}} = 0 \quad (12)$$

Now apply KCL at drain of M1 gives,

$$\frac{V_2}{r_2} + g_{m1}(V_{in} - V_{out}) - g_{mb1}V_{out} + \frac{V_2 - V_{out}}{r_{o1}} = 0 \quad (13)$$

Substituting Eq. (3.12) in (3.13) and writing $\frac{V_{out}}{V_{in}}$

$$\frac{V_{out}}{V_{in}} = \frac{g_{m1}r_{o1}}{1 + (g_{m1} + g_{mb1})r_{o1} + \frac{(r_2 + r_{o1})}{(r_1 || r_{o2})(1 + g_{m2}r_2)}} \quad (14)$$

With ideal current sources we get,

$$\frac{V_{out}}{V_{in}} = \frac{g_{m1}r_{o1}}{1 + (g_{m1} + g_{mb1})r_{o1} + \frac{1}{(1 + g_{m2}r_2)}} \quad (15)$$

Now by comparing Eq. (15) of super source follower with

Eq. (4) of simple source follower, it can be seen that the deviation of gain from unity is more in super source follower. Hence it can be concluded that the super source follower has little effect on open circuit voltage gain. The product of $g_m r_o$ for MOSFET is given by relation

$$g_m r_o = \sqrt{2\mu C_{ox} \left(\frac{W}{L}\right) I_d / \lambda I_d} \quad (16)$$

where, μ is mobility of charge carriers, C_{ox} is gate oxide capacitance, λ is channel length modulation coefficient and $\frac{W}{L}$ is aspect ratio. Here $\lambda \propto 1/L$, hence we get

$$g_m r_o \propto \sqrt{\left(\frac{WL}{I_d}\right)} \quad (17)$$

here, the width and length can be adjusted to get desired product without changing I_d .

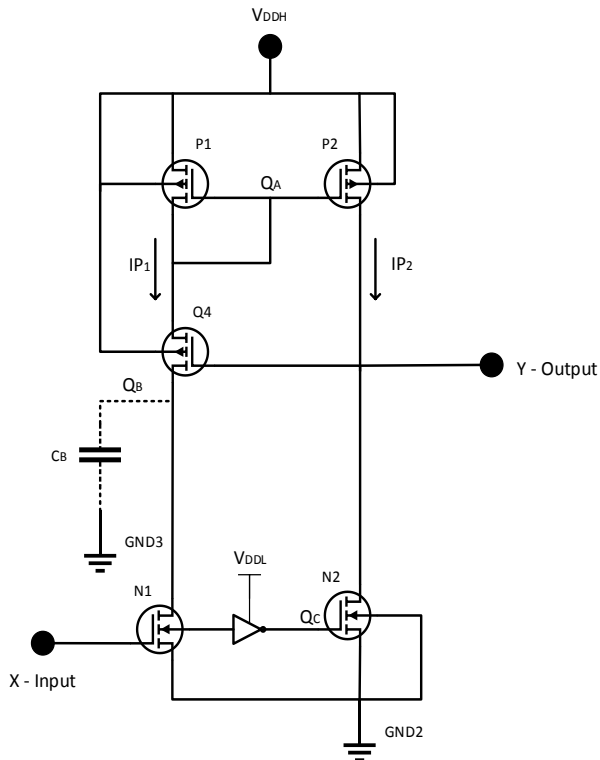


Fig. 7. Wilson Current Mirror level shifter circuit

In general, conventional level shifters consist of cross coupled PMOS and NMOS transistors driven by input signal. Consider a Wilson current mirror circuit shown in fig. Here when the input signal changes from “Low” to “High” then N2 turns OFF and N1 is turns ON and pulls the node Q_B down. Initially before transition the node the output signal had been low, causes P3 to be turned ON. As a result, a transition current flows between N1, P1, and P3. This transition current is mirrored to P2 resulting in pulling up the output node. When output node is pulled to V_{DDH} , P3 is turned OFF and therefore no current flows through N1, P1, and P3.

Similarly, when the input signal changes from “High” to “Low”, N1 turns OFF and N2 turns ON trying to pull the output node down. As a result, P3 is turned ON to charge Q_B , which is discharged to ground resulting in flow of transition current between P1 and P3 to charge node Q_B . When this current is mirrored to P2, it tries to pull down the output node. Due this there exists an increase in delay and power consumption of the circuit due to high to low transition circuit.

IV. PROPOSED LEVEL SHIFTER CIRCUIT

In order to reduce the drawbacks of the Wilson circuit mentioned in Fig 3, a source follower is proposed which act as level shifter. In source follower circuit, the load is replaced by MOS current source as shown in below Fig. 8.

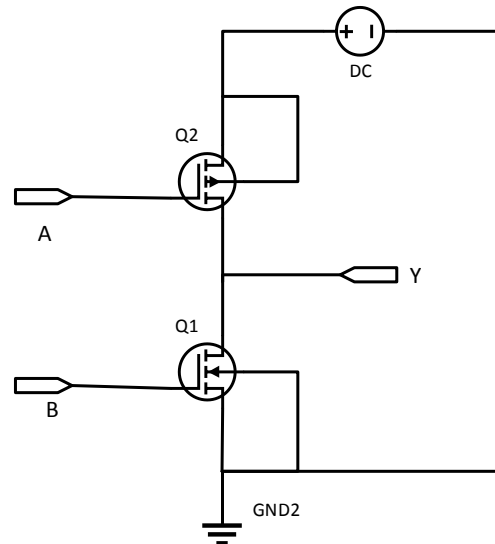


Fig. 8. Source Follower circuit

As the current source offers high resistance, the voltage applied across the N1 is the bias voltage V_{b1} . This bias voltage makes sure that the N1 MOS always operates in saturation region. In this circuit, the output voltage gain is approximately reduced and the power consumption is also less.

V. SIMULATION RESULTS

The circuit is simulated in Cadence virtuoso tool in 180nm technology. The supply voltage $V_{in}=1.8$ V and the maximum dc voltage considered is 2.5 V. The bias voltage is $V_{b1}=0.6$ V, the length and width of both NMOS and PMOS are considered as 180 nm, 2 μ m respectively. The results show that the voltage gain of the proposed circuit is less when compared to that of Wilson current mirror circuit. The analysis and graph of the proposed level shift circuit is shown below.

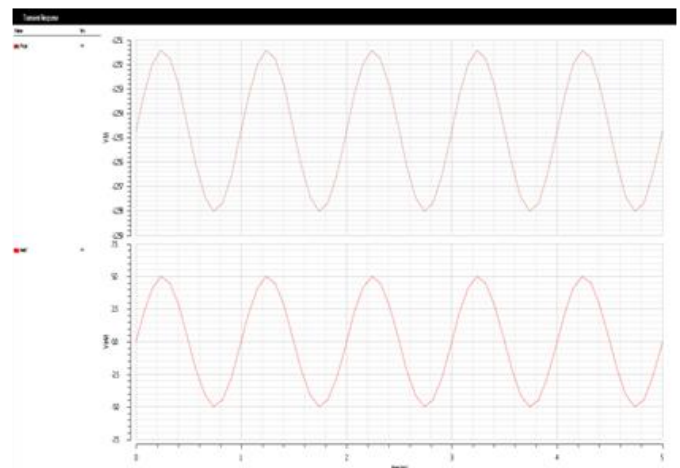


Fig. 9. Transient analysis of source follower

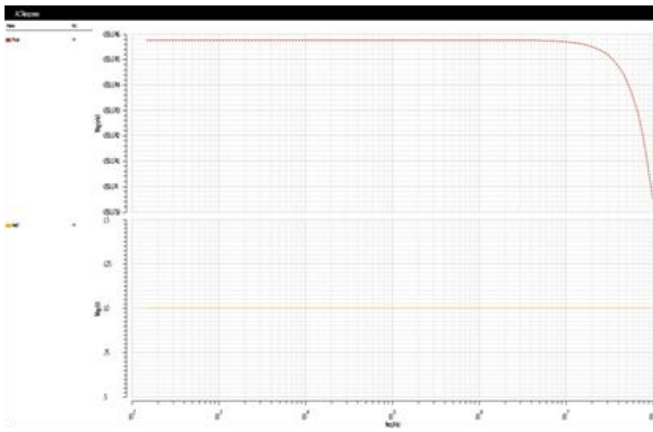


Fig. 10. AC analysis of source follower

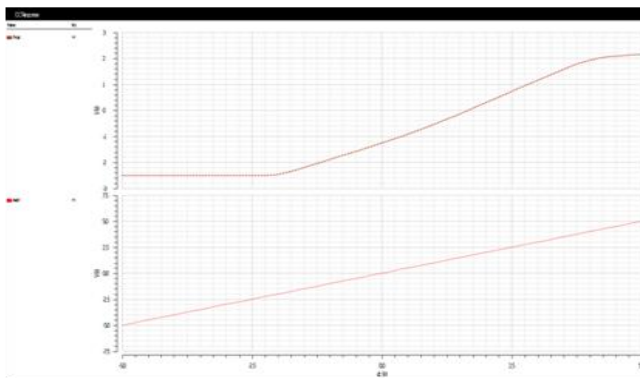


Fig. 11. DC analysis of source follower

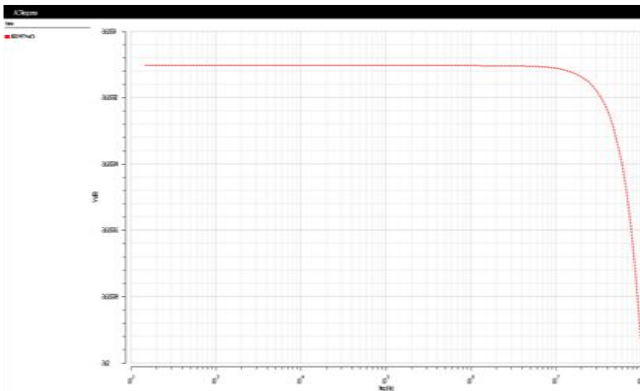


Fig. 12. Gain of source follower

VI. CONCLUSION

The main aim of this proposed circuit is to enhance the performance of a level shifter for low power applications and also reduces power dissipation in the circuit. The proposed configuration is simple and easy to implement. Simulations results have been verified using 180 nm technology and the results have been shown.

ACKNOWLEDGMENT

The authors would like to thank the management of NNRG Group of institutions for their motivation and

support. The authors thank their parents, teachers and friends for their unconditional love and support.

REFERENCES

- [1] K. Patkar and S. Akashe. "Design of level shifter for low power applications." In *Colossal Data Analysis and Networking (CDAN), Symposium on*, pp. 1-4. IEEE, 2016.
- [2] M. Lanuzza, P. Corsonello and S. Perri. "Fast and wide range voltage conversion in multi-supply voltage designs." *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 23, no. 2 (2015): 388-391.
- [3] M. Musab and S. Yellampalli. "Study and implementation of multi-VDD power reduction technique." In *Computer Communication and Informatics (ICCCI), 2015 International Conference on*, pp. 1-4. IEEE, 2015.
- [4] A. Shapiro and E.G. Friedman. "Power efficient level shifter for 16 nm FinFET near threshold circuits." *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 24, no. 2 (2016): 774-778.
- [5] M. Kumar, S. K. Arya, and Sujata Pandey. "Level shifter design for low power applications." *arXiv preprint arXiv:1011.0507* (2010).
- [6] M. Moghaddam, M. H. Moaiyeri and M. Eshghi. "A low-voltage level shifter based on double-gate MOSFET." In *Computer Architecture and Digital Systems (CADS), 2015 18th CSI International Symposium on*, pp. 1-5. IEEE, 2015.
- [7] R. Sharma and S. Akashe. "Analysis of low power reduction in voltage level shifter." In *Computational Intelligence on Power, Energy and Controls with their impact on Humanity (CIPECH), 2014 Innovative Applications of*, pp. 355-359. IEEE, 2014.
- [8] Q. A. Khan, S. K. Wadhwa and K. Misri. "A single supply level shifter for multi-voltage systems." In *VLSI Design, 2006. Held jointly with 5th International Conference on Embedded Systems and Design., 19th International Conference on*, pp. 4-pp. IEEE, 2006.
- [9] G. Srinivasulu, K. V. Ramanaih and K. P. Priya. "Design of Low Power High Speed Level Shifter." In *IJRET: International Journal of Research in Engineering and Technology*, pp.12-16. 2014.
- [10] Y. Haga and I. Kale. "Bulk-driven dc level shifter." In *Circuits and Systems (ISCAS), 2011 IEEE International Symposium on*, pp. 2039-2042. IEEE, 2011.
- [11] S. K. Manohar, V. K. Somasundar, R. Venkatasubramanian, and P. T. Balsara. "Bidirectional single-supply level shifter with wide voltage range for efficient power management." In *VLSI Design (VLSID), 2012 25th International Conference on*, pp. 125-130. IEEE, 2012.
- [12] K. Agarwal, V. Venkateswarlu, D. Anvekar and S. Basu. "A level shifter for Deep-Submicron node using multi-threshold technique." In *Recent Advances in Intelligent Computational Systems (RAICS), 2011 IEEE*, pp. 925-929. IEEE, 2011.
- [13] J. M. Lin, W. Y. Cheng, C. L. Lee, and R. C. Hsu. "Voltage island-driven floorplanning considering level shifter placement." In *Design Automation Conference (ASP-DAC), 2012 17th Asia and South Pacific*, pp. 443-448. IEEE, 2012.
- [14] W. M. Zheng, C. S. Lam, S. W. Sin, Y. Lu, M. C. Wong, U. Seng-Pan and R. P. Martins. "Capacitive floating level shifter: Modeling and design." In *TENCON 2015-2015 IEEE Region 10 Conference*, pp. 1-6. IEEE, 2015.
- [15] R. Matsuzuka, T. Hirose, Y. Shizuku, N. Kuroki and M. Numa. "A 0.19-V minimum input low energy level shifter for extremely low-voltage VLSIs." In *Circuits and Systems (ISCAS), 2015 IEEE International Symposium on*, pp. 2948-2951. IEEE, 2015.
- [16] K. H. Koo, J. H. Seo, M. L. Ko and J. W. Kim. "A new level-up shifter for high speed and wide range interface in ultra deep sub-micron." In *Circuits and Systems, 2005. ISCAS 2005. IEEE International Symposium on*, pp. 1063-1065. IEEE, 2005.
- [17] H. S. Gupta, S. Kirkire, S. Bhati, R. S. Chaurasia, S. Mehta, A. R. Choudhary, D. Patel and J. Vaghela. "Bipolar voltage level shifter." In *VLSI Design and Test (VDAT), 2015 19th International Symposium on*, pp. 1-5. IEEE, 2015.
- [18] S. Thakur and R. Mehra. "CMOS Design And Single Supply Level Shifter Using 90nm Technology." In *Conference on Advances in Communication and Control Systems*, pp. 150-153. 2013.

