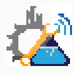

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Low-Power Programmable Pseudorandom Test Pattern Generators with Test Compression Capabilities

Indira Priyadarshini Gera
Department of Electronics and Communications Engg.
NNRG
Hyderabad, India

G.Bharathi Subhashini
Department of Electronics and Communications Engg.
Malla Reddy College of Engineering,
Hyderabad, India

Abstract — In this paper, a low-power programmable generator is proposed with a capability of producing required pseudorandom test patterns. The toggling levels and fault coverage gradients are adjustable in this work and are compared with the built-in self-test (BIST) based pseudorandom test pattern generators. To accomplish the objective of this paper a LFSR is tested with random variables and inputs and proved to be a better method as compared to the previous methods in the past. The proposed method could combine test compression with LBIST and both the systems could deliver high quality tests. Experimental results for the proposed design are reported herein with relevant outputs and expected outcomes.

Keywords—Gilbert mixer, low power, flicker noise, thermal noise, UWB.

I. INTRODUCTION

The role of pseudorandom test pattern generators (PRPG) are playing a key role in most of the digital designs to identify and rectify the problems associated with the integrated circuits. Most of the times PRPGs are considered to be built-in-test (BIST) generators and are very popularly used in most of the hardware circuit designs to establish the balance in terms of reliability and helps to reduce the maintenance cost [1]. The designs-for-testability techniques such as BIST help to place various testing functions physically with circuit under test (CUT). Three hardware blocks are needed for a BIST architecture which includes a) test pattern generator, b) response analyser and c) test controllers.

Generally, the pattern generators are some of the stored patterns such as counters, linear feedback shift registers (LFSR), etc. in a ROM; response analysers will be included with a comparator with variety of responses stored in it. An analyser will compact and analyze the test responses and verify the correctness of the CUT [2]. All these test and analysis responses will get activated by the test control block and plays a crucial role in most of the digital circuits. Digital systems are being tested and diagnosed for the entire lifetime at various occasions needs to be very quick and fault coverage must be very high. All these operations must be performed in most of the integrated circuits as system functions, hence, the name built-in-self test (BIST).

A. *Background Literature*

The research in the area of PTPG is being carried out since 90's after the evolution of IC's and various digital circuitries. Various testability analysis techniques were in the IC industry and in the initial stages some interactive techniques were used for modelling the circuit behaviour. A BIST analysis proposed by Carletta and papchristou was suitable for register transfer level (RTL) enables to correct the circuit modelling at the word-level correlation [3]. Considering the rapid growth in CMOS technology and increasing number of transistors within a unit chip area, the fault detection probability needs to be increased to overcome the random resistant faults. In order to detect such faults Favalli and Dalpasso used a weighted pseudorandom test generation (WPRTG) test sequence to characterize non-uniform distributions of various test vectors. The weights of such distributions will be identified after analyzing the CUT [4]. Later, reducing the power consumption techniques for PTPG was proposed by Murashko et al. for BIST and signature analyzers [5]. To improve the performance of PTPG a column-matching BIST was proposed by Fišer and Kubátová focused on reducing the size, i.e. portability and to increase the fault coverage [6]. In this method the authors used the WPRTG for fault coverage. Later a generalized linear feedback shift registers (GLFSR) was used by Wen-rong and Shu-zong to design a test pattern generator to cover high faults for a BIST design [7]. GLFSR is a combination of cellular arrays (CA) and linear feedback shift registers (LFSR). An encryption scheme for JPEG 2000 proposed by Hong et al. used a chaotic pseudorandom bit generator (PRBG) [8]. Cellular automata were used by Gao et al. for designing the test pattern generators and for response compaction in BIST system [9]. Later programmable PRPGs introduced by Tyszer et al. were suitable for the enhancing the fault coverage gradient and was suitable for low power applications as well [10]. This method can guide to generate a test sequence with improved fault coverage and pattern counts.

Strano et al. studied the methods to optimize the pseudo-random BIST for synchronous and multi-synchronous networks on chip [11]. Larger number of latencies was reported by applying this technique on on-chip interconnection networks. In an experiment carried out by Rani et al. used low hardware overhead with 3-

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weighted pattern generation for testing VLSI designs [12]. A pattern generator for BIST proposed by Ren and Xiong used a multi-polynomial LFSR for testing the faults and fault coverage covered using this method used less hardware with reduced cost [13]. The overall testing time using this method found to be very less as compared to earlier methods. Low-power programmable PRPG proposed by Filipek et al. have wide range of test compression capabilities [14]. This programmable PRPG is having the capability of generating test patterns with desired toggling levels and improved fault coverage gradients. Later, scan-based low power BIST based WPSPG along with reseeding was proposed by Xiang et al. supports both pseudorandom testing and deterministic BIST [15]. In the later case design-for-testability architecture can be slightly modified.

Now in this work, the focus is made on pseudorandom test pattern generators (PTPG) suitable for the digital IC applications at low power and high speed operations. The design aspects of PTPG must be addressed carefully in the present trend of CMOS technologies where the quest to reduce the size of transistor, improving the application performance and having multiple features within the portable devices has become a challenging trend. Therefore, the immense possibility to have complex circuitry and design errors in most of the digital circuits is quite evident since the evolution of digital circuits. Considering the above facts it is very important to have strict quality check at the time of designing and when the circuit is under operation. Various checking operations must be performed within the IC's for which the role of test pattern generation is critical. Most of the automatic test pattern generation (ATPG) methods used in electronic design automation use input sequence, which is applied at the input of the digital circuits. A comparison between correct and fault circuit behavior will be taking place using automated test equipments and the patterns generated will be useful for the testing purpose once the device is manufactured. Effectiveness of these PTPGs depends on the number of modeled defects, fault models, and detectable with the help of generated patterns. Higher the fault detection means better the testing quality and test application time depends upon the number of patterns tested within the defined time.

II. PROPOSED PTPG STRUCTURE

For the low power scan based BIST architecture and low power pseudorandom testing it is very much essential to have a suitable design-for-testability (DFT) architecture as shown in Fig. 1. The scan-forest architecture shown in Fig. 1 is used to test in first phase and individual stages of the phase shifter (PS) will drive the multiple chains [16]. This architecture is adopted to compress the test data and reduces to determine the volume of the test data. Different types of weighted signals $[e_0, e_1, \dots and\ e_n]$ will be assigned to scan chains in the initial phase, i.e. phase = 0. Each scan-in signal will help to drive the multiple scan chains and different weights are assigned to different scan chains. This method helps to reduce the size of phase shifter as compared to multiple scan-chain architecture.

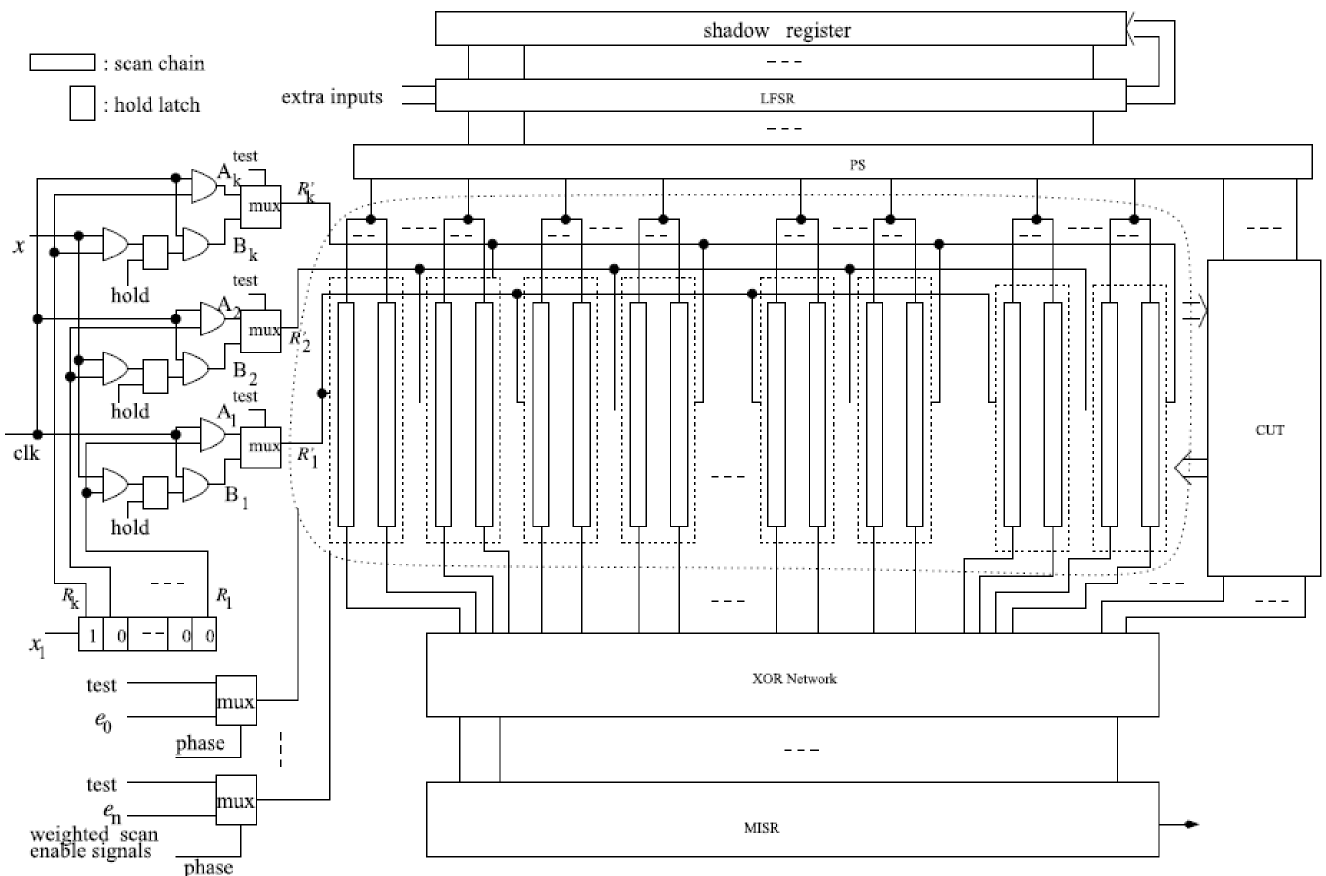

Fig. 1. DFT architecture for low power scan-based BIST

The LFSR size needs to be based on the maximum number of care bits of deterministic test vectors of BIST method. Sometimes the size may be very larger due to vectors with large number of care bits irrespective of well-designed phase shifters. Such situations will increase test data volumes to keep the seeds in order. By adding small number of extra variables to LFSR or ring generator this problem can be solved easily [15].

To design a PTPG we need to have a better LFSR structure, which in general depends on the characteristic polynomial. The number of flip-flops and non-zero coefficients will be based on the degree of polynomial (k). The number of XOR gates will be based on the non-zero coefficients and longest possible sequence for LFSR is given by $2^k - 1$ and it starts from the non-zero initial state. Longest possible sequence can be generated by using LFSR primitive characteristic polynomial only.

Each state of the LFSR will provide the essential patters for the CUT, where test per cycle cases are seen such as in the case of built-in logic block observer (BILBO). Higher fault coverage is provided by the LFSR if depths of pseudorandom patters are limited. However, LFSR produces serial bits of test patterns in the case of test-per-scan scheme. After this process test patterns are shifted and applied for CUT and the responses are loaded to scan registers followed by shifting process for compact of the bits for next patterns.

Now by assuming the k as the degree of the LFSR with a length of n for scan chain and $k < n$, the generated first pattern for each clock cycle only one new bit will be generating (i.e. the least significant bit). First pattern will be ready only after n clock cycles. That means n states are already passed and following patters will be generated in a sequence after every n clock cycles. Considering a LFSR with primitive characteristic polynomial as $P(x) = 1 + x + x^4$ for $k = 4$, the length of scan chain (n) will be equal to 6 and 5 test-per-scan cases will be there in a period of generated patterns [13].

In this work, the LFSR used two characteristic polynomials for the betterment of generating the pseudorandom patterns. Assume a 4-stage two polynomial LFSR as shown in Fig. 2 to understand proposed LFSR.

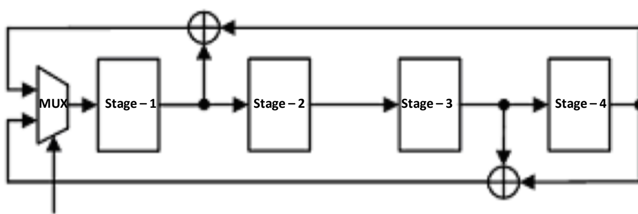

Fig 2. 4 – Stage two polynomial LFSR structure

Every bit in the test pattern will be applied to the 6-bit single chain and with characteristic polynomials as $P_1(x) = 1 + x + x^4$ and $P_2(x) = 1 + x^3 + x^4$. For the above two polynomials LFSR is more than 5 and pattern sequence generated by the Fig. 2 is shown in Fig. 3.

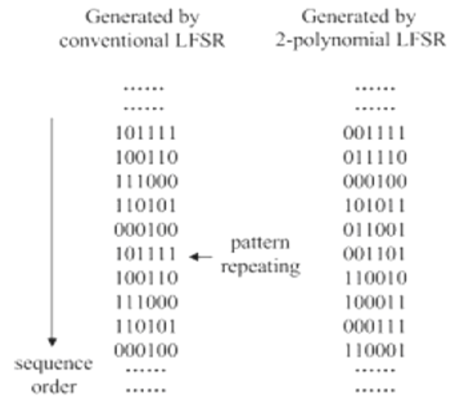

Fig 3. Pattern sequence with suitable example

Assuming f_i and g_i as the feedback coefficients of polynomials, the LFSR serial output sequence of a k stage as $\{x^1, x^2, \ldots x^k, x^{k+1}, \ldots\}$ gives the bits with the following expression:

$$x^{k+j+1} = \begin{cases} \sum_{i=j+1}^{j+k} f_i x^i, & j = 2 \times k \\ \sum_{i=j+1}^{j+k} g_i x^i, & j = 2 \times k + 1 \end{cases} \quad k \in Z^+$$

here x^1 is the firstly generated output and x^2 is the second output and so on.

In real-time the multi-polynomial LFSR will be almost similar to the conventional LFSR. In case of 2-stage LFSR, the multiplexer used will be of 2 to 1 and if the characteristic polynomial is greater than 2 means 3 to 1 multiplex will be used. However, multi-polynomial LFSR is proved to deliver better fault coverage in most of the pseudorandom patterns. Sometimes wrapping counter will be a useful hardware overhead and mixed-mode BIST is always a better option in the deterministic testing phases. Therefore in this work wrapping counter is used for pseudorandom testing phases. The characteristic polynomials used in this paper are as shown in Table I.

TABLE I. Used characteristic polynomials

Degree	Characteristic Polynomials
Proposed 5 stage	$P(x) = 1 + x + x^5$
	$P(x) = 1 + x^2 + x^5$
Proposed 5 stage	$P(x) = 1 + x + x^9$
	$P(x) = 1 + x^4 + x^9$
Conventional 8 stage	$P(x) = 1 + x + x^5 + x^6 + x^9$
Conventional 9 stage	$P(x) = 1 + x + x^4 + x^9$
Conventional 12 stage	$P(x) = 1 + x^4 + x^6 + x^9$

Now in low power applications it is very important to see that the hardware is reduced and hence the selecting the characteristic polynomial must not be larger as compared to the quarter of scan chain length. Also it is known that most the CUTs are involved with lots of

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combinational circuits and hence the primary inputs are determines the scan chain length of the CUT. Some of the CUTs are listed here for information: c432, c499, c1355, c1908, c2670, c5315, etc. Degree of convectional LSFR will not be more than 12 and the primary inputs will be even more than 200 in some of the combinational circuits [13].

In the proposed LFSR, initial seed selection is not critical and for each circuit number of experiments was performed with different LFSR stages and pattern depths by starting at same initial seed. With the acceptable pattern depths the LFSR seem to have higher fault coverage as compared to the conventional LFSR with degree 8 and only 62.5 % register stages are required to build the complete set up.

III. Low Power Pseudorandom Pattern Test Generator

In this work, a weighted PRPG for low power BIST is proposed as shown in Fig. 4 uses the gating technique.

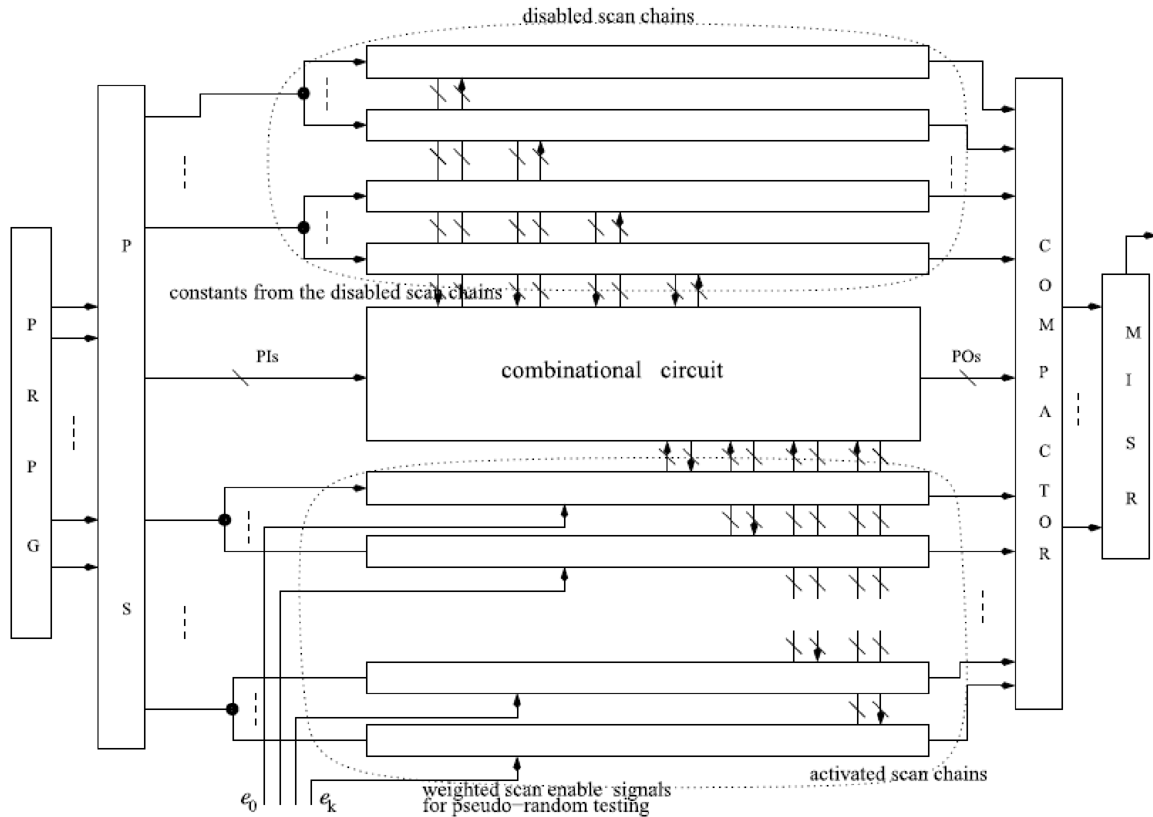

Fig. 4. Weighted Pseudorandom test generator for scan-tree based low power BIST

The gating technique helps to disable the excessive scan chains with constant values at the pseudo primary inputs (PPI). Scan chains in same scan trees will be selected into subsets of scan chains and are in general driven by the same clock signal. In this proposed method, weights for scan chains will be degraded in the sub-circuits and selects optimal weights for remaining scan chains in the subsets.

IV. Functioning of Weighted PTPG

The proposed method will be able to generate the degraded sub-circuits for all the subsets of scan chains. The PPIs are randomly assigned with designated values with 1 or 0 from the disabled scan chains. All scan flip flops with same level will be sharing same PPI and for the specified gates the inputs will be removed. Otherwise if there is a non-controlling value at the input, means a minimum of three inputs will be there in the main circuit. However, in the case of two input AND or OR gates with non-controlling inputs will be removed from the main circuit. In the case of NAND or NOR gates with non-controlling input values at any of the inputs means the gates will be degraded to an inverter. Similarly more than three inputs for XOR or NXOR gates means for the value of input value with 0 will be removed.

The architecture of scan-based BIST as shown in Fig. 4 will be having different weights of e_0, e_1,… e_k will be applied at the inputs as test-enable signals for a scan chain of SC_0, SC_1, … SC_k. In this method, randomly few constant values will be applied for all the scan flip flops in disabled scan chains. All these weights over test enable signals will be selected in degraded subcircuits. To avoid more capture cycles as compared to scan shift cycles, in this work the weights are not assigned with lesser than 0.5 to the test-enable signals. An efficient method was developed in this work to select the weights for test-enable signals of scan chain. Selections of the weights are determined by using testability gain function as given below:

$$G = \sum_{l/i \in F} \frac{|C'_1(l) - C'_0(l)|}{O'(l)}$$

here, l/i represent the stuck-at i ($i \in \{0,1\}$) at fault line l. The random-pattern resistant (F) is defined as a set of faults whose detection probability is no more than ten times that of the hardest fault. So using the above equation the testability gain function can be minimized.

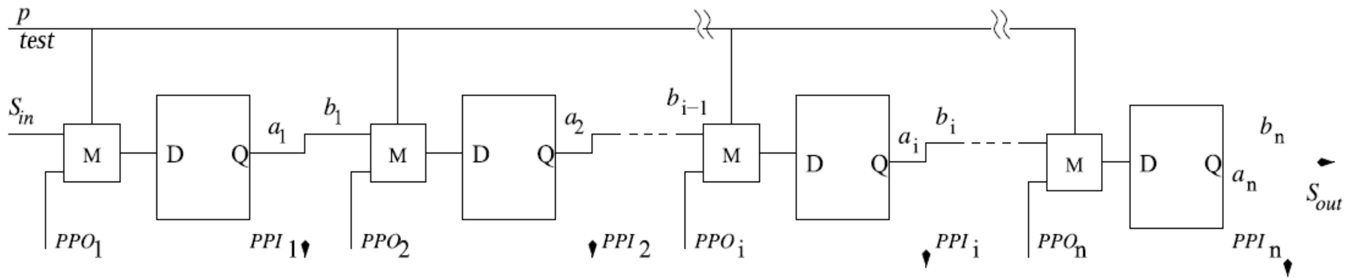

Fig. 5. The scan chain along with the weighted test-enabled signals

The weighted test-enable signals S_{in} and S_{out} are shown in Fig. 5. At the initial stages all the PPIs are assigned with a signal probability of 0.5 and pseudoprimary outputs (PPO) will be set to $\frac{1}{n}$.

The performance of the low power PRPG for circuits using netcard and vga with different percentages are calculated for the scan chains are shown in Fig. 6 and Fig. 7.

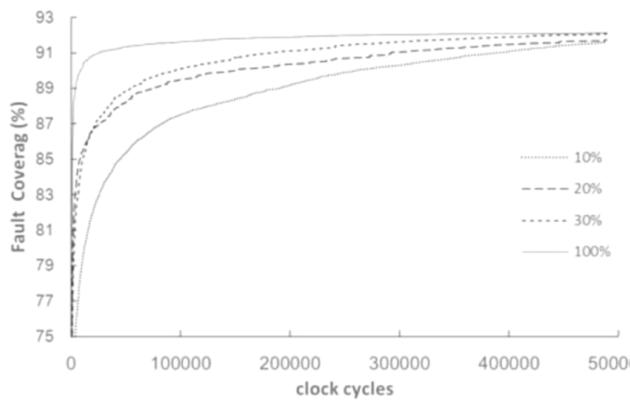

Fig 6. Fault Coverage with different toggle rates for vga-lcd

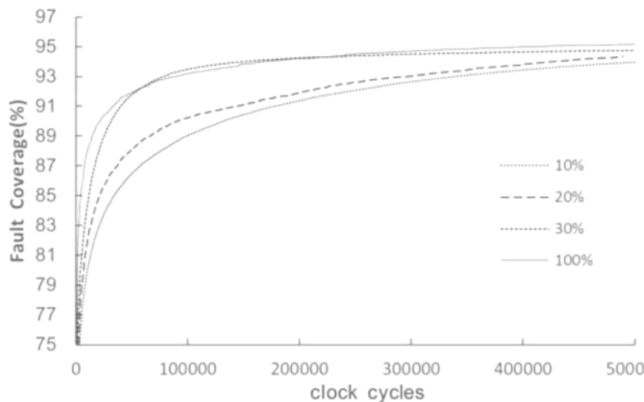

Fig 6. Fault Coverage with different toggle rates for Netcard

V. CONCLUSIONS

The proposed low power weighted PTPG will be working as follows. In the initial stages, first subset of the scan chains will be activated while the remaining scan chains are disabled. The pseudorandom pattern generated will be applied to the degraded subcircuits when scan chain was set to the capture cycles; otherwise note that the scan chain will be set to scan shift mode. Such a process will be continuing till the complete subsets of the scan chains are processed. This process will be continuing until all the clock cycles are completed.

The proposed low power weighted PTPG is capable of improving the fault coverage as compared with the conventional test-per-scan BIST approaches as per the experimental results. The overall test data to be stored has been reduced significantly using this method.

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