INTERNATIONAL JOURNAL OF RECENT TRENDS IN ENGINEERING & RESEARCH
Impact Factor 4.101 ISSN -2455-1457
RECENT ADVANCES IN ELECTRONICS & COMMUNICATION ENGINEERING (RAECE-2K17)

Printed Circuit Board design for Inverting Summing Amplifier using CADENCE

Anil Kumar Reddy Gattu
Department of Electronic and Communications Engg.
NNRG College of Engineering,
Hyderabad, India

MadhuShriramshetty
Department of Electronics and Communications Engg.
NNRG College of Engineering,
Hyderabad, India

***Abstract*—Cadence is the best Electronic Design and Automation (EDA) tool for PSPICE to check behavior of the any analogue or digital circuit and analyzing, Schematic of the circuit, pad stack creation for the selected component, footprint creation and PCB editing. This paper explains all the features of cadence with a basic amplifier such as PSPICE model of amplifier, transient analysis, Schematic of the amplifier and building of PCB for the same.**

Keywords—Cadencer,Electronic Design and Automation (EDA),PSPICE, Padstack, Footprint, PCB, Transient Analysis, Schematic, Amplifier.

I. INTRODUCTION

The cadence tool offers wide range of features in the analysis of any analogue or digital circuit. to schematic capture, simulation and PCB layout. OrCAD 17.2 PCB Designer with PSpice was used to design the PCB in this work. This suite comprises three main applications [5].

OrCAD Capture is a schematic capture application, and part of the OrCAD circuit design suite. Unlike NI MULTISIM, Capture does not contain in-built simulation features, but exports netlist data to the simulator, OrCAD. Capture can also export a hardware description of the circuit schematic to Verilog or VHDL, and netlists to circuit board designers such as OrCAD Layout, Allegro, and others.

- Capture includes a component information system (CIS), that links component package footprint data or simulation behavior data, with the circuit symbol in the schematic.
- Capture also includes a TCL/TK scripting functionality that allows users to write scripts, that allow customization and automation. Any task performed via the GUI may be automated by scripts.
- Capture can interface with any database which complies with Microsoft's ODBC standard etc. Data in an MRP, ERP, or PDM system can be directly accessed for use during component decision-making process

.**OrCAD EE PSPICE** is a SPICE circuit simulator application for simulation and verification of analog and mixed-signal circuits. PSPICE is an acronym for Personal Simulation Program with Integrated Circuit Emphasis.

OrCAD EE typically runs simulations for circuits defined in OrCAD Capture, and can optionally integrate with MATLAB/Simulink, using the Simulink to PSPICE Interface. OrCAD Capture and PSPICE Designer together provide a complete circuit simulation and verification solution with schematic entry, native analog, mixed signal, and analysis engines.

The PSpice Advanced Analysis simulation capabilities cover various analyses- Sensitivity, Monte Carlo, Smoke (Stress), Optimizer, and Parametric Plotter providing in depth understanding of circuit performance beyond basic validation.

The type of simulation performed by PSpice depends on the source specifications and control statements. PSpice supports the following types of analyses:

1. DC Analysis - for circuits with time–invariant sources (e.g. steady-state DC sources). It calculates all nodal voltages and branch currents over a range of values. Supported types include linear sweep, Logarithmic sweep, and Sweep over List of values.
2. Transient Analysis - for circuits with time variant sources (e.g., sinusoidal sources/switched DC sources). It calculates all nodes voltages and branch currents over a time interval and their instantaneous values are the outputs.
3. AC Analysis - for small signal analysis of circuits with sources of varying frequencies. It calculates the magnitudes and phase angles of all nodal voltages and branch currents over a range of frequencies.

The operating temperature of an analysis can be set to any desired value, and nodal parameters are assumed to be measured at a nominal temperature, by default 27 °C.

OrCAD PCB Designer is a printed circuit board designer application, and part of the OrCAD circuit design suite. PCB Designer includes various automation features for PCB design, board-level analysis and design rule checks (DRC).

The PCB design may be accomplished by manually tracing PCB tracks, or using the Auto-Router provided. Such designs may include curved PCB tracks, geometric

shapes, and ground planes. PCB Designer integrates with OrCAD Capture, using the component information system (CIS) to store information about a certain circuit symbol and its matching PCB footprint.

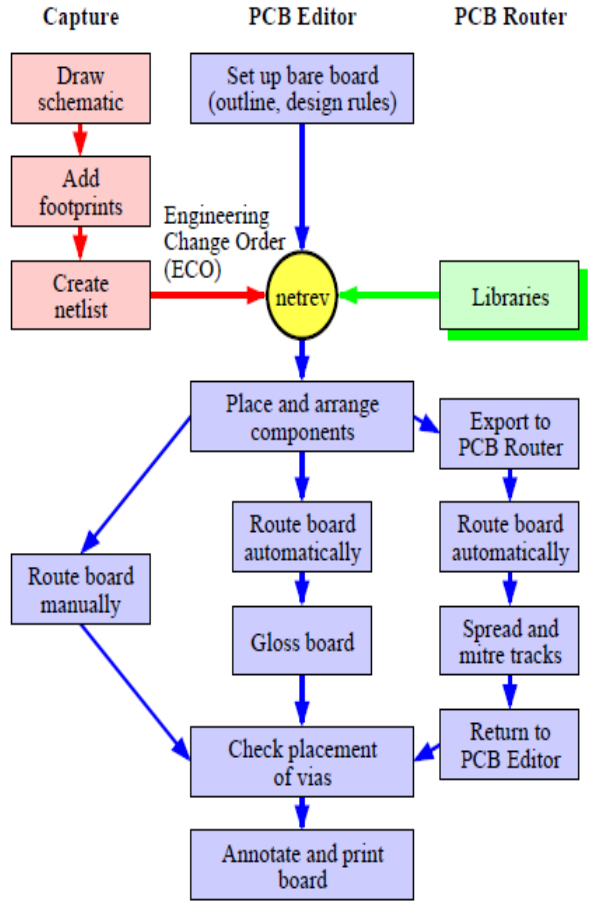

Fig. 1. Design flow for making a PCB with Capture and PCB Editor

II. INVERTING SUMMING AMPLIFIERCIRCUIT

Functioning of the cicuit

When the input signal Vin is positive, Op-Amp output terminal is negative, Diode D1 is reverse biased and D2 Diode is forward biased, the circuit is

$$Vb = -(R4/R5) * Vin$$

In the circuit, R1 and R2 have been chosen such that R4 = 2R5. So the voltage at Vb = -2Vin.

Thus during the positive half cycle of the rectified voltage Vb is applied to terminal B of the inverting summing amplifier is -2Vin. This inverting summing amplifier having two operational amplifiers with dc positive power supply of +12V, and negative power supply of -12V. positive feedback is provided to both operational amplifiers with 10KOhm and 1Kohm respectively. AC power supply is given as input source which is to be amplified. Here resistor R3 will be used as pull up resistor to improve the input signal strength.

The voltage at terminal A is Va = +Vin. The output from the summing circuit with R1=R2=R3 is Vo = –(Va+Vb). Hence Vo = -(Vin – 2Vin) = +Vin. So during the negative half cycle of the input, the Op-Amp output terminal goes positive, causing D4 to be reverse biased. Without D3 in the circuit, the Op-Amp output would be saturated in the positive direction. However, the positive voltage at the Op-Amp output forward biases the D3. This tends to pull the Op-Amp inverting terminal in a positive direction. But, such a move would cause the Op-Amp output to go negative. So, the output settles at the voltage close to ground level. So to be clear, the negative half-cycle is clipped off. That is Vb=0 and Va = -Vin. Totally the Vo will be $Vo = -(-Vin + 0) = +Vin$.

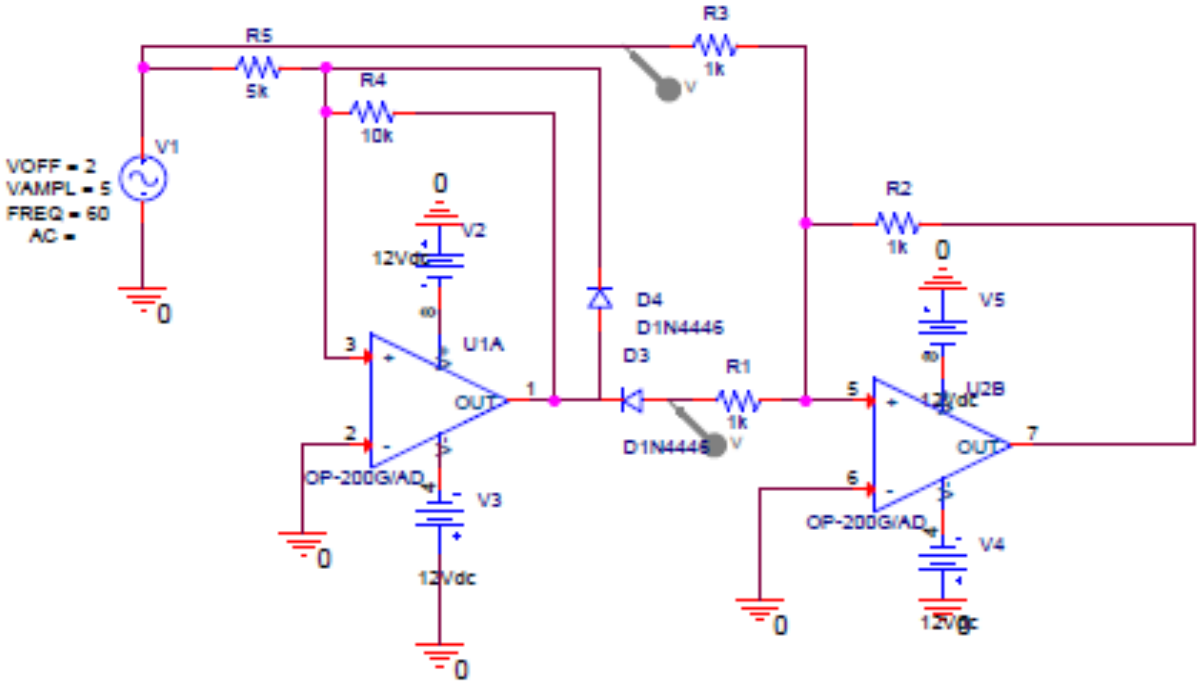

Fig. 2. PSPICE model of Inverting summing amplifier

III. ANALYSIS

For analyzing the circuit in PSPICE, Cadence electronic development and automation tool shall be used. In that tool most of the required components and spice models are readily available to use. If not found in the component database those can be downloadable from the web. First it is required to shortlist the components that are intended to use. Defining the property of each component and add the footprint in the properties section [3]. If footprint is not exist, then it is customizable to create own footprint that matches with the actual component.

Before analyze the circuit of the inverting summing amplifier need to follow the steps

1. place all the components having PSPICE models and make a circuit diagram.
2. Check for errors using DRC, electrical DRC and groundings.
3. Create new transient analysis for the circuit and run the simulator with necessary inputs.

When simulation is starting for transient analysis, the PSPICE checks for the all types of error such as floating points, design rule checker and PSPICE compatibility. Then it netlists all the components and generates a file with "netrev" extension. This file contains all the information of components and connections and values of each component, quantity with unique names[2].

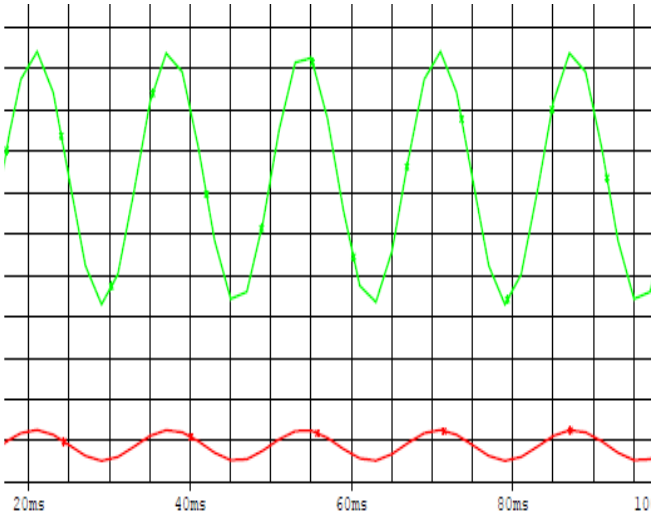

Fig. 3. Transient Analysis for the amplifier

In the first case it is known that the transient behavior of the circuit at ambient room temperature of 27°C which is default set up by the EDA tool. In the plot red line indicates the input sine wave and green line indicates the amplified signal output.

In the second case the transient analysis carried out at various temperature conditions. That means apart from the ambient room temperature, it is possible to estimate the performance of the give circuit at different temperature without subjecting the actual circuit to those temperatures.

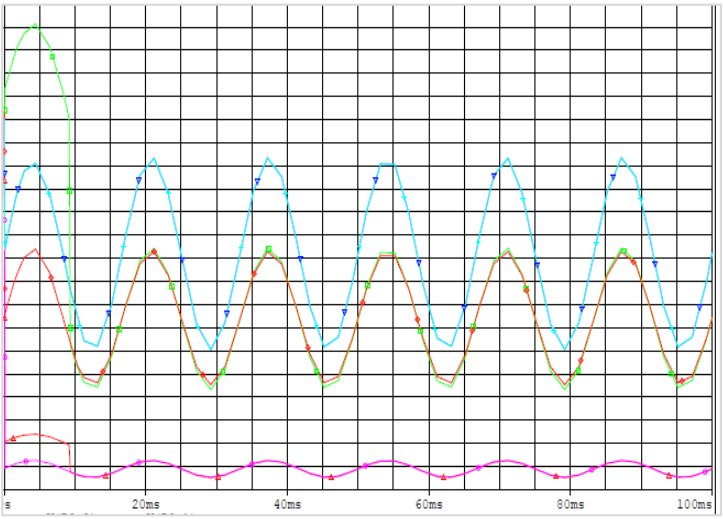

Fig. 4. Transient Analysis for the amplifier at temperatures 50, 70, 90°C

IV. PCB DESIGNING

A. *Classes and Types of PCBs*

The design approach for a PCB depends on many factors including its intended end use, design and fabrication complexity, acceptable fabrication allowances, and type of component and attachment technology. Standard classifications have been established to aid designers, fabricators, and consumers communicating with each other on these issues. The classifications include performance class, producibility level, and type of construction.

1. Performance Classes

PCBs can fall into any of three end-use performance classes. Throughout many of the IPC standards (IPC-7351, IPC-D-330, IPC-CM-770E) material performance and tolerance levels are determined by the class rating. Performance classes are based on things like allowed variation in copper-plating thickness, feature location tolerance, and hole diameter tolerance (plated and unplated), to name a few. The three classes are as follows:

Class 1, General Electronic Products, includes general consumer products like televisions, electronic games, and personal computers that are not expected to have extended service lives and are not likely to be subjected to extensive test or repair ability requirements [1].

Class 2, Dedicated-Service Electronic Products, includes commercial and military products that have specific functions such as communications, instrumentation, and sensor systems, from which high performanceis expected over a longer period of time. Since these items usually have a higher cost they are usually repairable and must meet stricter testing requirements.

Class 3, High-Reliability Electronic Products, includes commercial and military equipment that has to be highly reliable under a wide range of environmental conditions. Examples include critical medical equipment and weapons systems. They typically have more stringent test specifications and possess greater environmental robustness and rework ability.

2. Producibility Levels

Producibility levels are described in detail here. The levels are not a set of explicit requirements but a way of describing how complex a design is and the precision required to produce the particular features of a PCB or PCB assembly. Smaller features (trace widths, etc.) require stricter tolerances, which increases the design complexity. The IPC standards provide several tables that assist the designer in determining the complexity as it relates to SFAs.

Width tolerances are described in the standards. The three producibility levels are

Level A, general design—preferred complexity

Level B, moderate design—standard complexity

Level C, high design—reduced producibility complexity

B. PCB DIMENSIONS AND TOLERANCES

1. Standard Panel Sizes

Being aware of standard panel sizes may help reduce costs since smaller PCB designs can be panelized onto one large panel[4]. If you have flexibility in specifying the size of your board, you can do so in a way that will allow to maximize the number of boards on one panel. This helps reduce cost by minimizing the number of parts being handled and the amount of waste generated.

Table1. Standard Copper Clad Panel Sizes

	Number			
Letter	1	2	3	4
A	2.4 X 3.2	2.4 X 6.7	2.4 X 10.2	2.4 X 13.8
B	4.7 X 3.2	4.7 X 6.7	4.7 X 10.2	4.7 X 13.8
C	7.1 X 3.2	7.1 X 6.7	7.1 X 10.2	7.1 X 13.8
D	9.5 X 3.2	9.5 X 6.7	9.5 X 10.2	9.5 X 13.8
Sizes are given in inches.				

2. SMD Pad stack Design

A good pad stack promotes the best possible solder joint between a component termination (lead) and the PCB. The pad stack must allow for component dimensional variations, PCB fabrication tolerances, placement tolerances, and solder fillet specifications. Through-hole devices are relatively large and therefore more forgiving of these tolerances, but SMDs are typically much smaller and are therefore more sensitive to manufacturing and placement variations.

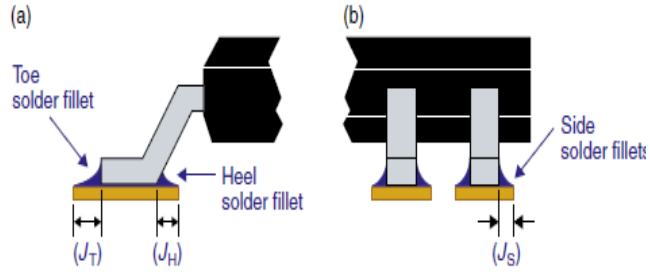

Fig.5. SMD padstack requirements: (a) sideview, (b) toe view.

$$W_{P(MAX)} = E_{MIN} - (E_{MAX} - 2L_{MIN}) + 2J_T + 2J_H + \sqrt[2]{(E_{TOL(\Delta)})^2 + F^2 + P^2}$$

$$H_{P(MAX)} = b_{MIN} + 2J_S + \sqrt{(B_{TOL(\Delta)})^2 + F^2 + P^2}$$

Whereas Wp is the width of the pad stack, Hp is the height of the pad stack, J_T is the toe solder fillet, J_H is the heel solder fillet, ETOL (Δ) is the tolerance of E, bTOL(Δ) is the tolerance of b, F is the PCB fabrication tolerance and P is the placement tolerance of pick-and-place machines.

3. Trough Hole Padstack Design

Through-hole devices fall generally into one of two categories: axial leaded or radial leaded. The foot print design for this type of device is determined strictly by the construction of the device. Clearly the pad stacks have to be located where the leads extend from the body. Radial leaded devices include pin grid arrays and many discrete transistor devices such as TO220 and T092 packages. The only variable is the pad stack design with regard to the lead diameters. The regular passive elements such as resistor, capacitor and inductor, pull up resistor network, input and output terminals through hole packages of ICs uses the through hole pad stacks to design the actual footprint of those components. But most common footprints commonly used are available in the library.

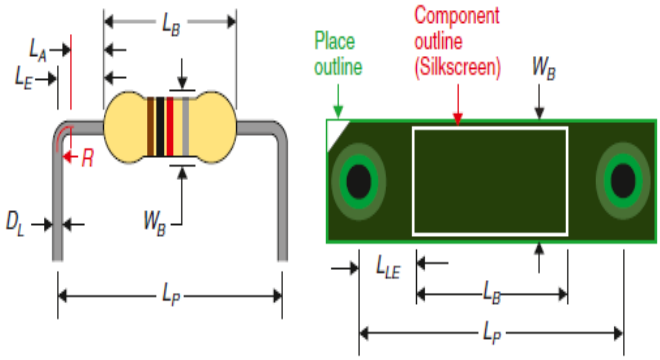

Fig.6. Generic footprint designparameters for axial leadedcomponents.

$$LP = LB + 2(R + LA)$$

Where LP is the pad spacing (centre to centre), LB is the length of the body, R is the bend radius allowance, and LA is the length of the lead extension from the end of the body to the beginning of the bend. R and LA are dependent on the diameter of the lead, DL, and that L E is the sum of L A and R.

$$DH = (DL + 2TP)Xk,$$

Where DHis the diameter of the drill hole in Pad stack Designer, DLis the diameter of the lead (per the component's data sheet or by measurement), TPis the thickness of the plating inside the hole (and k is a user defined tolerance factor, for which 1.05 <k _<3.0 (1.5 is recommended).

Pad stacks define every aspect of how a component's pins will be fastened to the PCB and how traces will be connected to them. Pad stack definitions specify areas for copper pads on outer and inner routing layers, thermal reliefs and clearance areas in plane layers, openings in solder masks, and solder paste (optional). From the PCB

designer's perspective, the drill hole may also be considered part of the pad stack definition, but the copper used to plate through holes and vias is not. This is because the plating thickness is controlled by the board manufacturer and is typically insignificant relative to the drill and lead diameters.

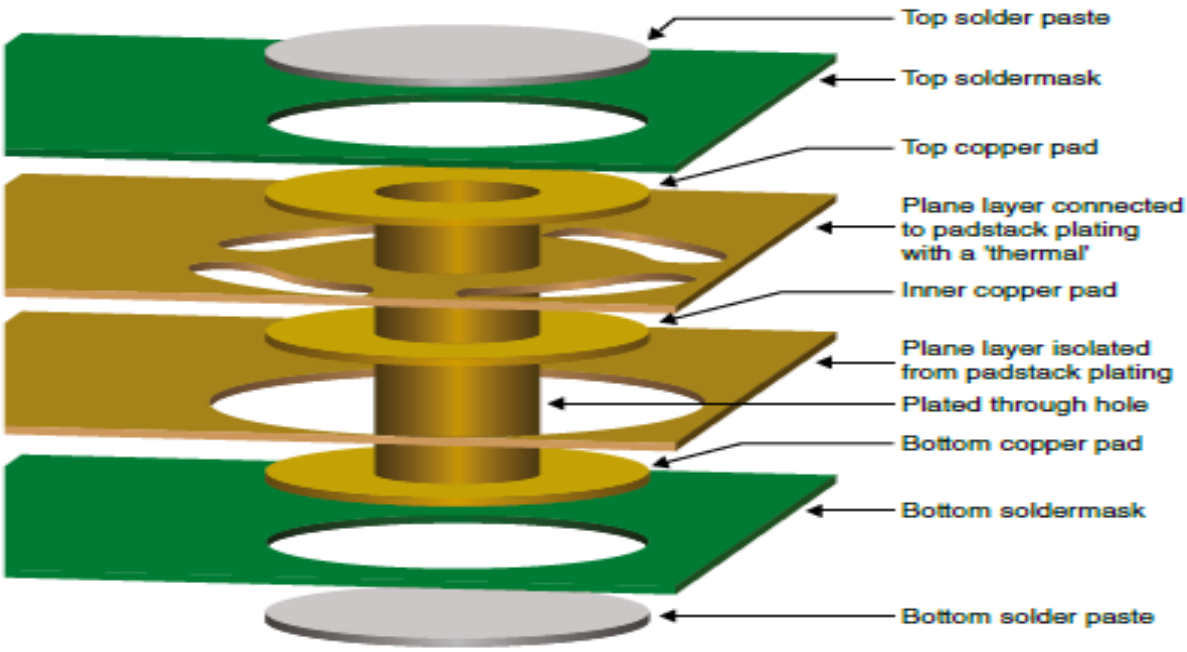

Fig. 7. Elements of a pad stack from the PCB perspective

1. **Regular pads**: The values on the internal layers can be identical to the outer layers but often they are slightly smaller (anywhere from 0 to 20 mils difference in diameter depending on the size).
2. **Thermal reliefs**: The native padstacks in the symbols library typically use circles that are the same size as the antipad. Circles work for positive planes but not for negative planes. For negative planes you need to use Flash symbols. Flash symbols are described later, so for the time being leave the thermal relief as a circle. The procedure for defining padstacks that have no thermal reliefs (i.e., completely connected to a plane) is described later.
3. **Antipads**: The clearance between a pad (or hole) and the surrounding copper (e.g., on a plane layer) should be similar to or larger than the trace spacing constraints you will likely use in your design. A typical clearance diameter is 10 to 20 mils larger than the pad diameter. Note that, if an inner pad much smaller than the outer layer pads, the antipad on the inner layer should still be larger than the largest pad in the padstack, otherwise undesirable capacitive coupling can occur between the larger pad and an adjacent plane layer.
4. **Soldermasks**: Soldermask openings are usually a little larger than the outer pads so that registration tolerance errors will not cover any of the pad. The exact amount really depends on the capabilities of your board manufacturer, but in general the soldermask opening is typically 10 to 20 mils larger than the outer pads.

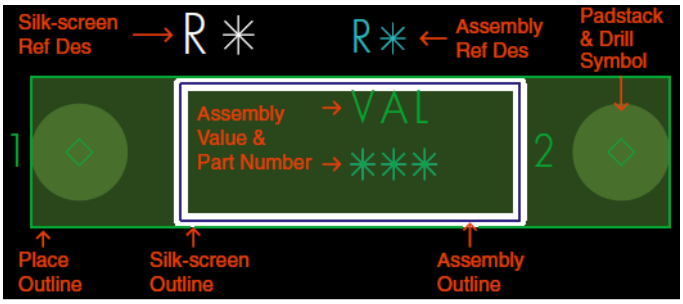

Fig. 8. THD Footprint of the resister

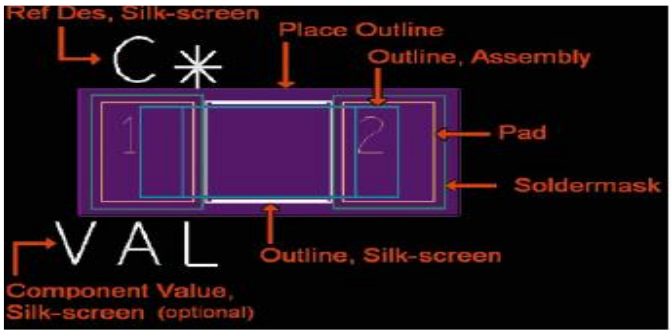

Fig. 9. SMD Footprint of the capacitor

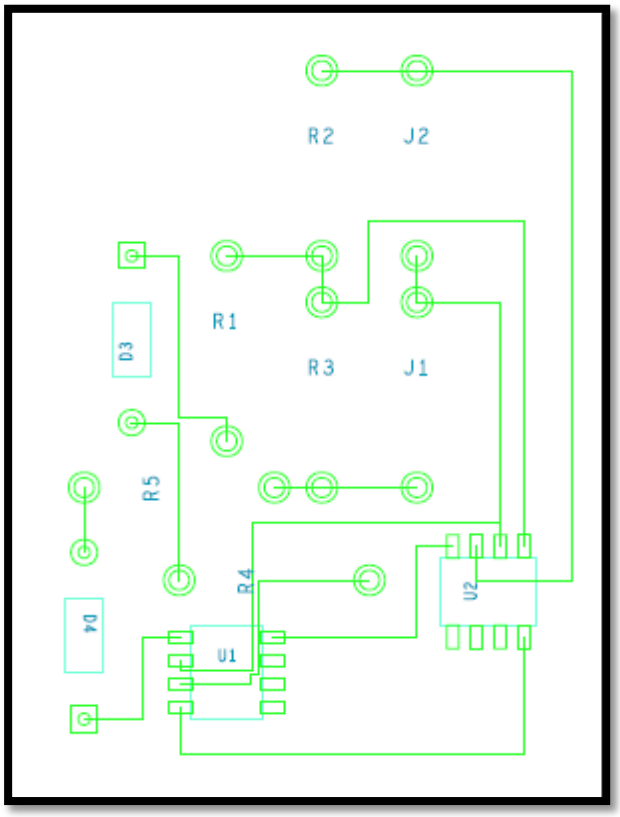

Fig. 10. PCB top view of the Amplifier

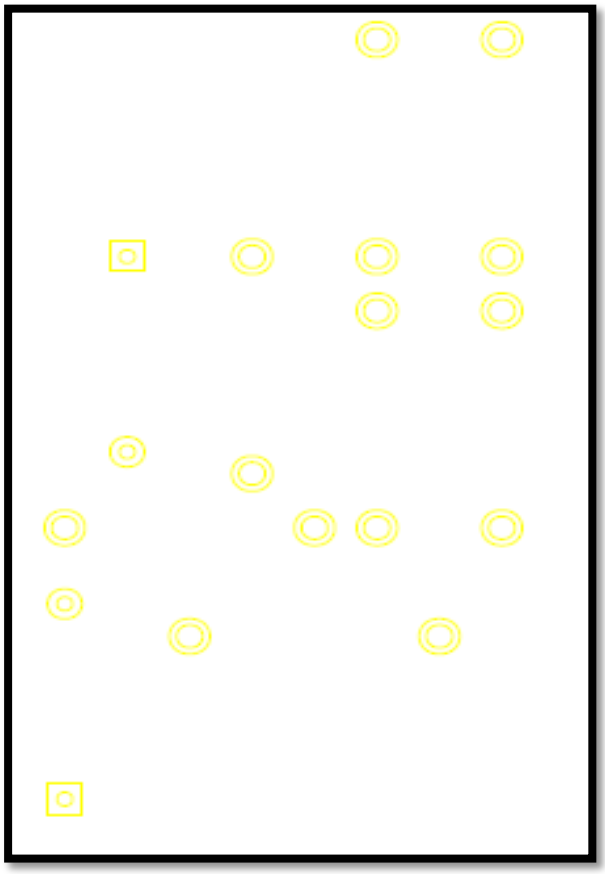

Fig. 11. PCB bottom view of the Amplifier

Allegro PCB builder allows to place all the foot prints in a predefined area called PCB board with rated thickness. After placing all the footprints routing of paths between components can be done. There are two types of routing. One is auto route in which allegro tool will automatically root the paths between the components with best possible. On the other end in manual mode user to place the paths with low occupying space and best shortest route to decrease the cost of production [6][7]. After completion of routing process that file is to save as board file with the ".brd" extension

V. Conclusions

The inverting summing amplifier is used in precision wave rectifiers to achieve better gain margins. Implementing the circuit in cadence PSPICE tool helps to understand the circuit in better way, to know the actual practical challenges to implement the same in actual case by considering all possible aspects of the circuit by its properties and working. In this paper it is clear that the amplification of the circuit is dependent of temperature factor.

While building the PCB for the amplifier circuit, Design rule checker notifies every point to point errors or warning list that may be affect the possibilities of building of the PCB. PCB is editable in the cadence Allegro tool. Running this tool helps to estimate the size of the PCB, thickness, packing density, cost and also properties of PCB.

Acknowledgment

The authors would like to thank P. Sampath Kumar for his motivation and great support. The authors thank their parents and teachers for their unconditional love and support.

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