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# Single Chip ASIC Design For Wireless Sensor Networks

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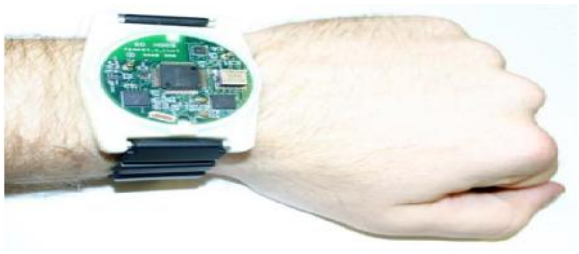
**Abstract:** This paper describes the hardware requirements and design constraints that derive from unique features of body sensor networks (BSNs). Based on the BSN requirements, we examine the tradeoff between custom hardware and commercial off the shelf (COTS) designs for BSNs. The broad range of BSN applications includes situations where either custom chips or COTS design is optimal. For both types of nodes, we survey key techniques to improve energy efficiency in BSNs and identify general approaches to energy efficiency in this space.

**Keywords:** body sensor networks; sub-threshold circuits; wearable computing; energy efficient design

## 1. Overview of BSNs

A confluence of advancements in diverse areas of research, including device integration, energy storage, sensor technology, and wireless communications, have facilitated the creation of body sensor networks (BSNs). BSNs like TEMPO are helping clinicians improve healthcare assessment accuracy and precision for better diagnosis, treatment, and assistance of movement disorders.

**Figure 1.** TEMPO packaged (cover removed) and wrist mounted.



For life-critical applications that require continuous high fidelity sensed data for real-time assessment and intervention (e.g., fall

detection, heart arrhythmia detection, *etc.*), which would be very costly to transmit wirelessly, reduction or elimination of wireless transmission may be necessary to meet longer battery life and wearability requirements. Such applications may need to make intervention/actuation decisions on-node and only employ wireless transmission when events of interest are detected. This system level design decision will help to reduce node power consumption sufficiently to satisfy the other system requirements. BSNs for delay insensitive applications, such as those employed by clinicians to gather information in large volume, may alternatively leverage lower power on-node storage, rather than wireless transmission, to increase battery life. Such store-and-forward use cases, including Holter monitoring and activity logging, are capable of acquiring high fidelity data for later assessment off-node. In such cases, on-node processing is limited, as more resource rich or expert assessments are made off-node. Finally, real-time applications involving wireless transmission and high fidelity data (e.g., gait analysis, activity monitoring, gaming, *etc.*), combine on-node signal processing with radio management to meet battery life demands of hours to days.

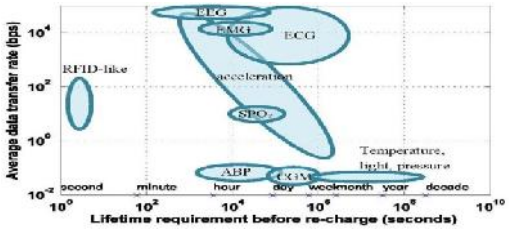
**Figure 2.** Broad design space for BSN, but size limits energy for all applications.

Value to the user will ultimately determine each technology's success. BSNs must effectively transmit and transform sensed phenomena into valuable information and do so while meeting other system requirements, such as energy efficiency. The value of a BSN therefore rests in large part on its ability to selectively process and deliver information at fidelity levels and rates appropriate to the data's destination, whether that is to a runner curious about her heart rate or a physician needing a patient's electrocardiogram. These disparate application requirements require the ability to aggregate hierarchical information and integrate BSN systems into the existing information technology infrastructure. Increased value of the BSN to the user will also increase user tolerance of non ideal wearability or other technological difficulties.

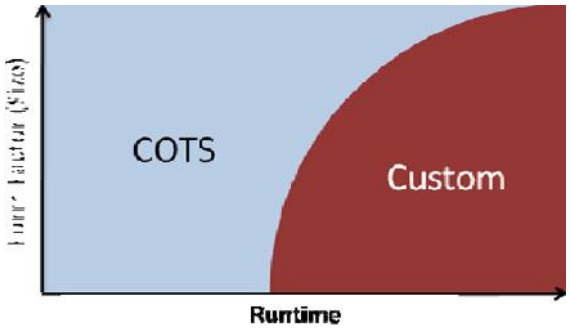
In this paper, we describe methods for developing efficient hardware within the unique set of requirements of BSNs for different parts of the BSN application design space. Due to the ubiquitous and strict energy constraint on all BSNs, we focus on energy efficiency. In addition, the approaches for achieving energy efficiency in BSNs designed with COTS components sometimes differ from those designed with custom hardware, and this paper explores both paradigms. Finally, this analysis is done within the context of current and projected BSN applications and use cases.

## 2. Hardware Selection—Commercial off the Shelf or Custom?

As we will describe in more detail in Section 3, flexible hardware is inherently less efficient than hardware targeted for a specific application.




Considering the broad range of requirements in Figure 2 combined with a strict energy constraint, there is little hope for a single system




platform to support the full range of applications. General purpose sensing platforms like the motes of the WSN community are typically too large in size or onsume too much power to meet application requirements in the BSN domain.

**Figure 3.** Hardware design space for COTS *versus* custom circuits

single chip ASIC design due to the fundamentally different manufacturing processes required for MEMS *versus* electronics. BSN sensors that measure acceleration may need to incorporate multiple ASICs or a mixture of ASICs and COTS.

The final decision between a custom design *versus* a COTS design must account for the previous points combined with the economics of the intended application. Designing a COTS system is orders of magnitude faster and cheaper than building a custom IC based node, and COTS nodes provide excellent solutions in many lower lifetime BSN scenarios. For example, low volume research platforms or nodes intended for short term clinical monitoring applications may be more

economically produced via a COTS design. In such applications, the final device operational characteristics are much less well defined, and engineering costs are ongoing. In this case the economies of reducing such costs via the employment of a flexible platform outweigh the benefits of extra efficiency that an ASIC solution would offer. For example the TEMPO3 system mentioned in Section 1 may be reprogrammed to operate in a clinical environment in which continuous data streaming is a requirement, or in a more longitudinal study in which data may be stored on node and offloaded after an extended measurement session. Additionally, COTS devices have steadily been improving in computing performance. When TEMPO1 was introduced in 2006, the processor employed had 48 kB of flash memory, 2 kB of RAM, and operated at a maximum clock frequency of 8 MHz. There are now available pin compatible drop-in devices from the same family that have over 100 kB of flash, 8 kB of RAM, and are capable of operating at 20 MHz within similar power budgets. This clearly leads to an expanded application space for a given sensing technology, with little or no non-recurring engineering (NRE) costs for hardware design. High volume, single purpose, mass market devices favor ASIC approaches in which the NRE costs are amortized over many units. Even if COTS systems provide a weaker solution (e.g., by limiting lifetime) than ASICs, simple economics will make COTS the better choice for many BSN applications that cannot provide the volume required to justify an ASIC solution.

## 3. General Strategies for Energy Efficient BSN Hardware

We have emphasized that many design decisions depend on the specific BSN application in question, but we can also identify general strategies that should influence any BSN design. In this section, we examine several key tradeoffs that affect BSN design and that provide important opportunities for saving energy regardless of the specific BSN application. Specifically, we examine balances between on-node computation and communication, flexibility and efficiency, and data fidelity and energy consumption. Before describing these tradeoffs, we introduce supply voltage management as a means of energy minimization in circuits, which provides an important foundation for custom energy efficient circuit design of energy constrained systems like BSNs.

### Supply Voltage Management

Lowering the supply voltage to a circuit is a well known approach for reducing energy. In this section, we first discuss the limit of lowering voltage to reduce energy consumption, and then describe how dynamic voltage scaling can allow us to tradeoff energy and performance.

For digital circuits, energy of computation varies as the square of the supply voltage ($V_{DD}$), which makes it desirable to operate at the lowest possible voltage while preserving functionality and meeting

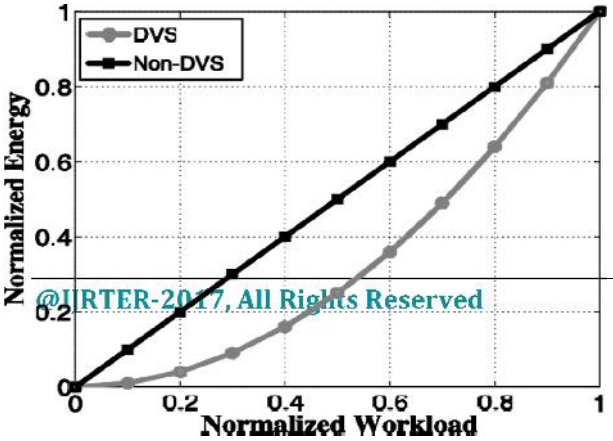
timing constraints. Taking this principle to the extreme, we observe that sub-threshold (sub-$V_T$) operation of digital integrated circuits provides one important option for energy efficient processing. Sub-$V_T$ circuits use a $V_{DD}$ that is below the threshold voltage, $V_T$, of the transistors. This makes the transistors “off” by conventional definitions, but the change in transistor gate-to-source voltage ($V_{GS}$) produces a difference in sub-$V_T$ conduction current that allows static digital circuits to operate robustly, although slower than they

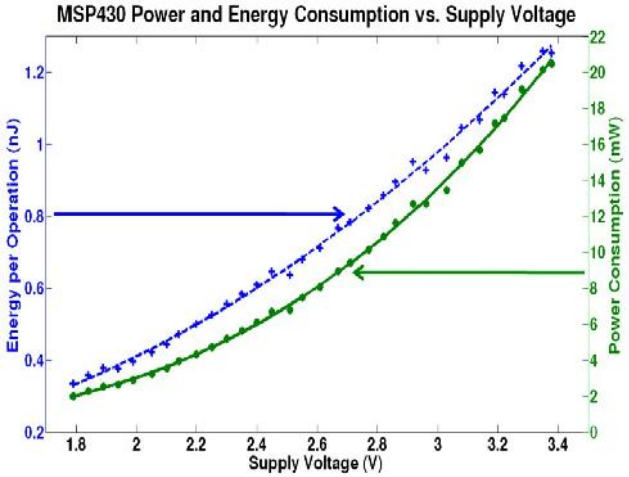
would be at higher voltage. The lower speeds are still more than sufficient for many BSN operations (up to 10's of MHz). Both the off-current and the on-current of the transistors vary exponentially with $V_{DD}$ in the sub-$V_T$ region ($V_{GS} < V_T$). Nevertheless, the on-current in sub-$V_T$ remains larger than the off-current by enough (1000× or so) to enable proper functionality of the digital gates. Due to the quadratic relationship between energy and $V_{DD}$, the main advantage of sub-$V_T$ operation is a reduction in energy consumption of over 10× compared to traditional circuit implementations. In fact, sub-$V_T$ operation has been shown to minimize energy per operation in conventional CMOS circuits [6]. For this reason, sub-threshold operation will play an important role in custom hardware for BSNs.

There are some challenges to making sub-$V_T$ digital circuits work. Most notably, the reduced $I_{on}/I_{off}$ ratio combines with process variations in the threshold voltage to increase the potential for circuit failure. Sub-$V_T$ circuits also must be level converted to interface with super-$V_T$ design, such as radios or sensors. Additionally, design of sub-$V_T$ circuits is not yet commonplace. Standard cells used in designs are rarely designed for this voltage of operation, in which transistor strengths change. Nevertheless, sub-$V_T$ operation is an emerging approach that is very useful for BSN nodes[7].

**Figure 4.** Energy-workload curve of normal operation and dynamic voltage scaling (DVS).




Operating at a low voltage all of the time may not be a viable option for all BSNs, because lower voltages slow down circuit speed. Given that a BSN's processing latency and throughput




requirements may change during execution in response to real-time data and mode changes, dynamic voltage scaling (DVS) can be employed to minimize $V_{DD}$ given those requirements. When high performance is necessary to meet system level requirements, the circuits can operate at the energy-costly higher voltage level. By reducing the circuit's $V_{DD}$, quadratic energy savings can be achieved instead of just the linear savings obtained through power gating (Figure 4). Different DVS schemes propose different approaches to scaling in terms of the circuit topology and interval at which the voltage is changed, and the overhead of most schemes are minimal compared to the energy savings accomplished, especially when that scaling includes dropping to sub-$V_T$ levels when permissible [8].

Some COTS chips provide built-in DVS capabilities or allow for development of DVS schemes. For instance, the TI MSP430 and other similar microcontrollers (MCUs), have on-board clock generation hardware that allows the MCU to programmatically change the operating clock frequency. This is

accomplished in the MSP430 through the use of a Digitally Controlled Oscillator (DCO) that may be calibrated using a low frequency (32 kHz) watch crystal as a reference. Frequency agility is accomplished by switching different programmable constants into two clock control registers. The actual change in clock frequency occurs within approximately 10 µs. Furthermore, this microcontroller operates over a wide range of voltages. The clock oscillator may be varied over a 16 to 1 range and the supply voltage over a 2 to 1 range. Within this envelope, a combination of processing rate and power requirements exist, making COTS embedded processors of this type ideal candidates for inclusion in a DVS scheme for BSNs. Figure 5 shows potential DVS operating points measured for the MSP430F2131 processor as explored in [9].

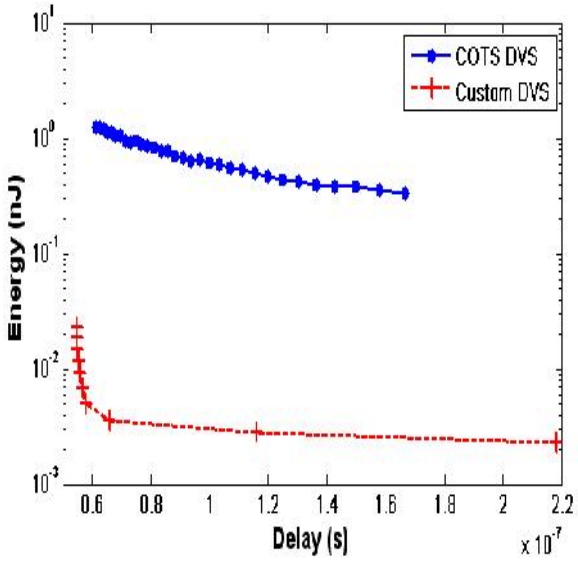
**Figure 5.** Operating points for a COTS MCU [9].

For longer lifetime BSN applications where the savings from Figure 5 are still inadequate, a similar DVS scheme can apply to a custom chip. Figure 6 compares a custom MCU design [7] to the MSP430. The custom design offers a 100× improvement in energy per instruction. However, this does not come free of tradeoffs. In this case, the custom built MCU does not have its own clock generation hardware, and frequency agility is not as straight forward since there is only one, single frequency main clock. Though this custom designed MCU also operates over a wide range of voltages and is capable of supporting DVS, additional design effort is required to build in these operating modes. What's more, custom designed hardware does not enjoy the complete suite of mature and compatible peripherals as COTS components, which degrades custom hardware's flexibility.

**Communication versus Computation**

As is the case in most WSNs, wireless transmission of sensed data is the largest power consumer in most current BSNs [9]. This problem is particularly acute in medical BSN applications, in which sensor data rates may be high relative to many WSN applications. Figure 7 illustrates this relationship with the COTS TEMPO platform as an example, where the high power consumption of the Bluetooth transceiver swamps the low power consumption of the TI MSP430 microcontroller during raw data transmission. We could improve this situation by using a lower power radio (e.g., COTS implementing a different protocol, or a custom design), by duty cycling and sending data in bursts, or by other strategies. In this section, however, we focus on the strategy of using computation on the node to reduce the cost of communication, which can influence all types of BSN design regardless of hardware choice.

**Figure 6.** TEMPO 3.1 power consumption breakdown (with gyroscopes off).




Significant power reduction can be

achieved through the development of on-node signal processing and data management which can dramatically reduce the number of bits to be transmitted. By reducing the number of bits to transmit, we effectively allow more substantial duty cycling of the radio (e.g., leaving it off for a larger fraction of the time). Methods to reduce communication data include traditional compression along with advanced signal processing techniques such as pattern classification and feature detection algorithms. Low power signal processing therefore becomes increasinglyimportant to BSN power efficiency.

## 3. Conclusions

In this paper, we have explored strategies and methodologies for energy efficient design of BSN nodes. Starting from the characteristics of BSNs that arise from their application space and make them unique (including significant differences from traditional WSNs), we have identified the tradeoff metrics available for design optimization. We then elaborate on general strategies for designing energy efficient hardware, focusing on the tradeoffs of computation *versus* communication, flexibility *versus* efficiency, and data fidelity *versus* energy. We examine key tradeoffs in the BSN space that ultimately may lead to the decision between a COTS based platform or a custom IC design. Finally, we present two cases of previous work to show examples of a COTS based node and a custom designed hardware node. As the field of BSNs continues to grow, we anticipate that a rich selection of design techniques will lead to creative solutions leveraging both types of hardware design and resulting in numerous successful BSN deployments.

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