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COMPARATIVE ANALYSIS OF 4-BIT MULTIPLIER CIRCUITS

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ABSTRACT

A fast and energy-efficient multiplier is always needed in electronics industry especially digital signal processing (DSP), image processing and arithmetic units in microprocessors. Multiplier is such an important element which contributes substantially to the total power consumption of the system. Multipliers of various bit-widths are frequently required in VLSI from processors to application specific integrated circuits. Recently reported logic style comparisons based on full-adder circuits claimed complementary pass transistor logic (CPL) to be much more power-efficient than complementary CMOS. The most important and widely accepted metrics for measuring the quality of multiplier design propagation delay, power dissipation and area. This paper describes the comparative performance of 4-bit multipliers designed using MICROWIND, using domino logic style.

1. INTRODUCTION

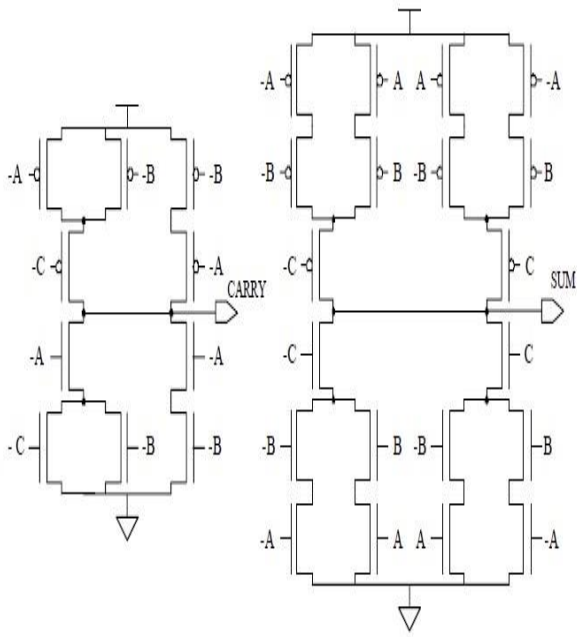
The increasing demand for low-power very large scale integration(VLSI) can be addressed at different design levels, such as the architectural, circuit, layout and the process technology level. At the circuit design level, considerable potential for power savings exists by means of proper choice of a logic style for implementing combinational circuits.This is because all the important parameters governing power dissipation-switching capacitance, transition activity, and short-circuit gggg choosen logic style. Depending on the application, the kind of circuit to be implemented, and the design thechnique used, different performance aspects become important.

2. LOGIC DESIGN STYLES

Bisdounis et al. Has proposed a large number of CMOS logic design styles. For multiplication adder is used as a basic element. For arithmetic applications, following three different logic styles are used for a full adder design to achieve best performance results for multiplier design.

2.1 CONVENTIONAL STATIC CMOS LOGIC-CSL

The recent VLSI arithmetic application i.e. 4-bit RCA, uses conventional static CMOS logic. The schematic diagram of a conventional static CMOS full adder cell is illustrated below



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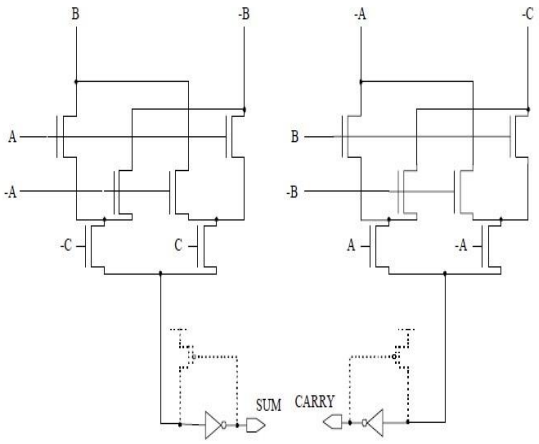
The signals noted with '-' are the complementary signals.

2.2 Complementary Pass-transistor logic-CPL

The basic difference of pass-transistor logic compared to the CMOS logic style is that the source side of the logic transistor networks is connected to some input signals instead of the power lines. The advantage is that one pass-transistor network(either PMOS or NMOS) is sufficient to perform the logic operation, which results in a smaller number of transistors and smaller input loads, especially when NMOS networks are used.



2.3 Pseudo NMOS logic

Gain ratio of n-driver transistor to p-transistor load is important to ensure correct operation. Accomplished by ratioing the n and p transistor sizes.

2.4 Dynamic CMOS LOGIC

Pull-up time improved by virtue of the active switch (p-transistor can be much larger). Pull-down time increased due to the ground switch. During cascading these structuring, the delay in the discharging of the left-most n-logic block at the start of the evaluate phase.

2.5 CMOS domino logic

These structures can be cascaded. In a cascaded set of logic blocks, each stage evaluates and causes the next stage to evaluate. It is widely used in high-performance microprocessors. It requires simulation.

3. MULTIPLIERARCHITECTURES

The wide-bit addition is vital in many applications such as ALUs, multiply-and accumulates (MAC) units in DSP's and versatile microprocessors. It is also important for the performance of direct digital frequency synthesizers (DDFSs) where it is used as a phase accumulator. Numerous multiplier implementations exist whereas some are good for low power dissipation and some takes least propagation delay.

3.1 Array multiplier

An array multiplier is very regular in structure as shown in figure. It uses short wires that go from one full adder to adjacent full adders horizontally, vertically or diagonally. An nxn array of AND gates can compute all the a_ib_i terms simultaneously. The terms are summed by an array of 'n[n-2]' full adders and 'n' half adders. The shifting of partial products for their proper alignment is performed by simple routing and does not require any logic.

The number of rows in array multiplier denotes length of the multiplier and width of each row denotes width of multiplicand. The output of each row of adders acts as input to the next row of adders. Each row of full adders or 3:2 compressors adds a partial product to the partial

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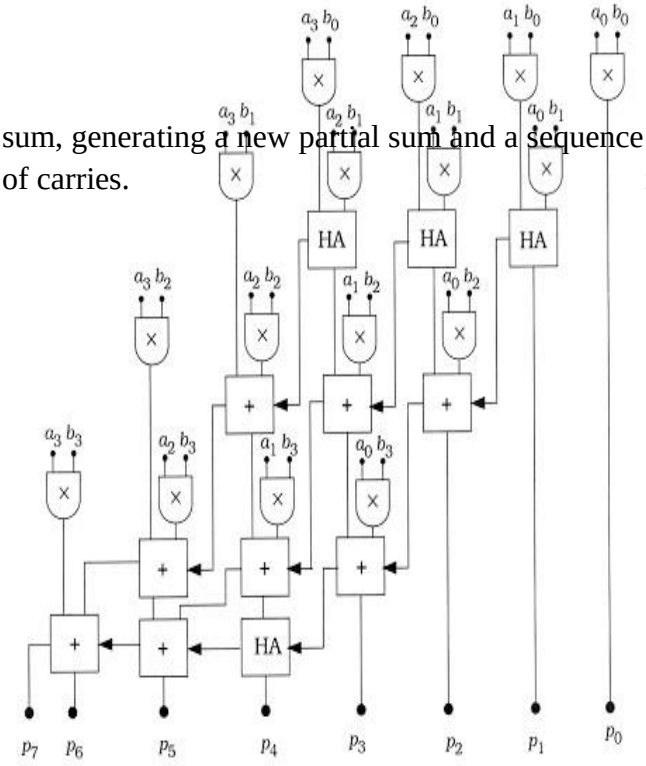

The delay assoaciated with the array multiplier is the time taken by the signals to propagate through the AND gates and adders that form the multiplication array. Delay of an array multiplier depends only on the depth of the array not on the partial product width. The advantage of array multiplier is its regular structure. Thus it is easy to layout and has small size. In VLSI design, the regular structures can be tiled over one another. This reduces the risk of mistakes ans also reduces layout design time. This regular layout is widely used in VLSI math co-processors and DSP chips.

3.2 Tree multiplier

C.S.Wallace suggested a fast technique to perform multiplication in 1964. The amount of hardware required to perform this style of multiplication is large but the delay is near optimal. The dealy is proportional to log(N) for column compression multipliers where N is the word length. This architecture is used where sum, generating a new partial sum and a sequence of carries. speed is the main concern not the layout regularity.

This class of multipliers is based on reduction tree in which different schemes of compression of partial product bits can be implemented. In tree multiplier partial-sum adders are araanged in a treelike fashion, reducing both the critical path and the number of adders.

4.PERFORMANCE PARAMETERS AND SIMULATION SET-UP

The 4-bit multipliers are compared based on the performance parameters like propagation delay, number of transistors and power dissipation. To achieve better performance, the circuits are designed using CMOS process. All the circuits have been designed using MICROWIND. The power estimation is a difficult task because of its dependency on various parameters and has received a lot of attention. Direct simulation method is used to analyse the results. The comparative results for two different 4-bit multipliers for different logic design styles.

5. VEDIC MULTIPLIER

Multiplication are extensively used in Microprocessors, DSP and communication applications. A higher order multiplications, a huge number of adders are to be used to perform the partial product addition. The need of low power and high speed multiplier is increasing as the need of high speed processors are increasing. The vedic multiplication technique is based on 16 vedic sutras or aphorisms, which are actually word formulae describing natural ways of solving a whole range of mathematical problems. The mathematical operations using, vedic method are very fast and requires less hardware, this can be used to improve the computational speed of processors. This paper describes the design

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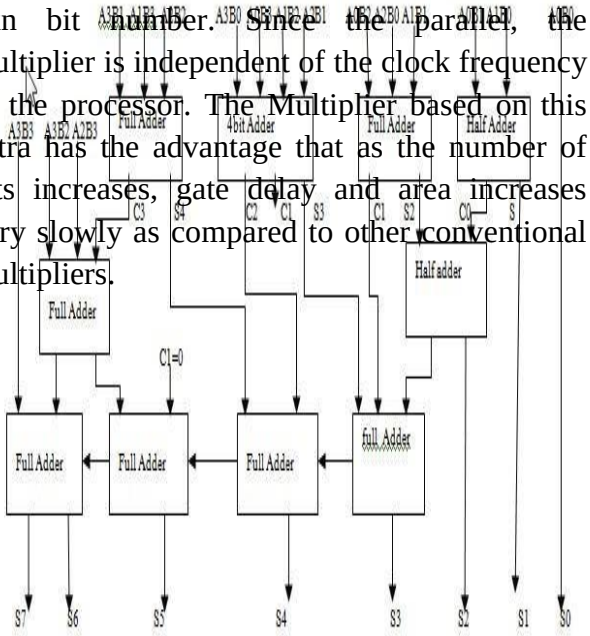
and implementation of 4X4 vedic multiplier based on Urdhva-Tiryakbhyam sutra (vertically and crosswise technique) of vedic mathematics using number system.

4.4 Vertical and crosswise technique

The proposed Vedic multiplier is based on the "Urdhva Tiryakbhyam" sutra (algorithm). These Sutras have been traditionally used for the multiplication of two numbers. The use of Vedic mathematics lies in the fact that it reduces the typical calculations in conventional because the Vedic formulae are claimed to be based on the natural principles on which the human mind works. Vedic mathematics is a methodology of arithmetic rules that allow more efficient speed implementation. It also provides some effective algorithms which can be applied to ideas to the binary number system to make the hardware. It is a general multiplication formula it means 'vertically and crosswise'. It is based on a partial products can be done with the concurrent be generalized for nxn bit number. Since the parallel, the multiplier is independent of the clock frequency of the processor. The Multiplier based on this sutra has the advantage that as the number of bits increases, gate delay and area increases very slowly as compared to other conventional multipliers.



The y multiplier is very regular in structure as shown in figure. It uses short wires terms are that go from one full adder to adjacent full adders horizontally, vertically or diagonally. An nxn array of AND gates can compute all the a_ib_i terms simultaneously. The terms are summed by an array shifting of partial products for their proper alignment is performed by simple routing and does not require any logic. The number of rows in array multiplier denotes length of the multiplier and width of each row denotes width of multiplicand. The output of each row of adders. Each row of full adders or 3:2 compressors adds a partial product to the partial sum, generating a new partial sum and a sequence

A3 A2 A1 A0 ×B3 B2 B1 B0

A3B0 A2B0 A1B0 A0B0
A3B1 A2B1 A1B1 A0B1 +

A3B2 A2B2 A1B2 A0B2 +

A3B3 A2B3 A1B3 A0B3 +

P7 P6 P5 P4 P3 P2 P1 P0

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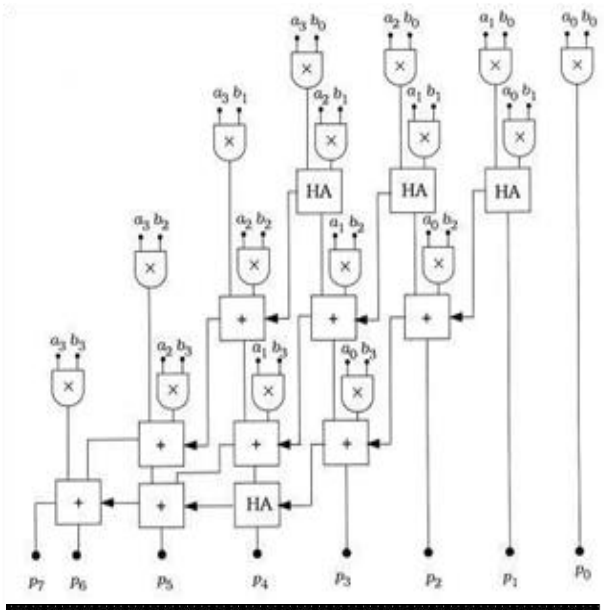

The delay associated with the array multiplier is the time taken by the signals to propagate through the AND gates and adders that form the multiplication array. Delay of an array multiplier depends only upon the depth of the array not on the partial product width.

RESULT ANALYSIS

It has been observed that 4*4 Vedic multiplier is better than 4*4 Array Multiplier. It helps a person to solve problems faster. It provides one line answer. Time saved can be used to answer more questions. It better in terms of Propagation Delay, Average Power Consumed and Power Delay Product(PDP). In terms of propagation delay in Vedic multiplier by using CMOS logic styles is 0.40ns and In Array multiplier Propagation Delay is 25.3ns.As a conclusion 4*4 Vedic Multiplier is better than Array multiplier in terms of Propagation Delay i.e. fastest circuit operation.

CONCLUSION

It can be concluded that the performance of the 4x4 bit Vedic multiplier seems to be highly efficient interms of speed when compared to Array multipliers. Reducing the time delay is very essential requirement for many applications and Vedic Multiplication technique is very much suitable for this purpose.

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