DIFFERENTIAL CONDITIONAL CAPTURING FLIP-FLOP TECHNIQUE USED FOR LOW POWER CONSUMPTION IN CLOCKING SCHEME

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Abstract—A novel Differential Conditional Capturing Flip-Flop (DCCFF) for low power and high performance applications is presented in this paper. Conditional capturing flip-flop eliminates the redundant internal transitions and it operates with a sinusoidal clock. The sinusoidal clock is utilized by reduced swing inverters at the clock port. By applying the power gating to the DCCFF the low-power consumption is achieved. Power gating technique doesn’t supply current to blocks that are not in use.

Keywords-component: low power, High-performance, Flip-Flop, Power gating

I.INTRODUCTION

In many digital Very Large Scale Integration circuit (VLSI) design which consists of clock distribution network, latches and flip-flops is one of the most power consuming components. Latches and flip-flops have direct impact on power consumption and these are sequential elements. Latch is a level triggered and it has one value. Flip-Flop is an edge triggered and it has two values. The advantageous factors in the flip-flops are high speed, low power consumption, less number of transistors, less internal activity when data activity is low. By reducing the both clock power and Flip-Flop power we can reduce the total power consumption. Clock signal is a sine wave produced by the clock generator (or) clock distribution network.

The clock distribution network is used to distribute the clock signal and it consumes 50-60% of power. The buffer in the CDN acts as a holding area, used to insert delays, strengthens a signal so that it can be fanned out with integrity. Any amplifier is a buffer and it consumes 30-35% of power. The clock buffers have better balance between rise and fall time. Full time is equal to time for a waveform to fall from 90% to 10% of its steady state value and Rise time is equal to time for a waveform to rise from 10% to 90%. The clock tree network have high impedance interconnects that decay clock signal strength and their major drawback is their power dissipation. Power dissipation means energy is dissipated (or) lost from electrical system. The large amount of capacitance driven by the clock network results in higher power dissipation. To reduce power dissipation in clock network it is necessary to maintain the dynamic, static, leakage and short-circuit current. The total power dissipation can be described by, 

\[ P_{\text{avg}} = P_{\text{dynamic}} + P_{\text{short-circuit}} + P_{\text{leakage}} + P_{\text{static}} \]

P dynamic= CL*V*N*F and it is proportional to the load capacitance CL, square of Vdd, switching activity and clock frequency. The dynamic power consumption is caused by the switching activity of the circuit (or) charging and discharging of capacitances in the circuit. During charging the output node makes a full transition from 0 to Vdd and an amount of energy from the power supply is dissipated as heat. During discharge phase no power is drawn from the power supply. The higher operating frequency leads to more switching activities in the circuit and it results in increased power dissipation. The dynamic power is the dominant factor compared with the other components of power dissipation and it is reduced by the reduction of the average number of transitions per clock cycle or switching activity or reduces the clock frequency. Short - circuit Power is caused by the current flow through the direct path existing between the power supply and the ground during the transition phase which means that when the input signal changes from 1 to 0 and 0 to 1 there exists a small time interval this results in the short circuit current flows between the power supply and ground. The short- circuit power is also caused by switching of transistors.

The low source -drain potential difference also results in small short-circuit current. By maintaining the proper rise and fall time throughout the clock tree reduces short circuit power. Leakage current is caused by two types one is reverse-bias diode leakage current at the transistor drains and other is sub threshold current. The reverse-biased diode leakage occurs because of transistor is getting off and current increases with increases in temperature. Diode formation is inherent and results in leakage current. Sub threshold leakage current occurs due to carrier diffusion between the source and drain. The magnitude of the sub threshold current increases when the gate to source voltage is smaller than threshold voltage and it results in the power dissipation of sub threshold leakage. The leakage problem mainly appears in very low frequency circuits or ones with sleep modes and it is several orders of magnitude smaller than the dynamic power. The leakage current techniques are applied at low-level design abstraction such as process, circuit and circuit design. The static power dissipation is the product of the leakage current and supply voltage. Static current depends on the logic state of its output and reversing the signal polarity for minimizing the probability of static current flow. The static current is reduced by transistor sizing.

Resonant Clocking enables the generation of clock signals with reduced power consumption. It uses the
LC tank to drive the clocks. The LC wave has equal phase and magnitude. Power consumption refers to the electrical energy applied to the electrical appliances to maintain its operation and it affects the high performance designs. By reducing the flip-flop power we can reduce the power consumption. The flip-flop power can be reduced by the reduction of transistor count and reducing redundant internal transitions.

Conditional capturing is used to minimize power at low data switching activities. Power gating technique is presented in this paper to achieve low power. Power gating technique is used to reduce power consumption by not supplying the current to the block which doesn’t operate. Some of the power gating parameters are power gate size, power gate leakage, gate control slew rate and switching capacitance. The power gate size handles the switching current. In power gate leakage power gates are made of active transistors to reduce leakage and it leads to power saving. In gate control slew rate we can calculate the efficiency. The Switching capacitance can be switched several times and it doesn’t affect the power. By reducing the transistor gate to source voltage power gating reduces leakage.

In coarse-grained power gating sleep transistors are coarsely placed. Coarse-grained power gating is also be implemented by the Ring-based (or) column-based manner depending upon application. In Ring-based, Power gates are switched off as a ring and power signals are turned on using the special corner cells. In column-based, power gates are arranged in column manner. When the power is switched in this method it is disconnected from all logic and it results in the loss of states. To preserve the state it should be stored. The main advantage of Coarse-grain sleep transistor is it shares charge and discharge current and it provides more flexibility. Power gating reduces leakage by reducing transistor gate to source voltage. The operation of the power gating is simple.

In active mode, virtual voltage is acting as power supply at a potential of Vdd to the Block, leakage power exists in both header and this circuit block. In standby mode it switches off the header and the virtual voltage drops. So it results in the less voltage.

This paper is organized as follows. Section II represents the description of conditional capturing flip-flop. Section III presents the power gated conditional capturing flip-flop. Section IV includes the simulation results and performance comparison. The conclusion of this paper is provided in section V.

II. DIFFERENTIAL CONDITIONAL CAPTURING FLIP-FLOP

Conditional capturing is a low-swing flip-flop and by using the low swing voltage on the clock distribution network we can reduce the clock power. Conditional capturing flip-flop eliminates unnecessary redundant internal node transitions to minimize power at low data switching activities.

The schematic diagram of the Differential Conditional Capturing Flip-Flop is shown in figure1.
Fig 1 Differential Conditional Capturing Flip-Flop

The main advantage of DCCFF is that there is no speed penalty. The sinusoidal clock signal is applied to the node of reduced swing inverters to reduce short circuit power. In reduced swing inverters the first pMOS transistor is the load pMOS transistor and it reduces the voltage at the source of other pMOS in each inverter.

When the clock signal applied to the gate of the nMOS transistor (MN1) which is connected to ground is able to pull down SET/RESET latch. MP1 and MP2 called pMOS transistors used to charge the SET/RESET nodes. Conditional capturing technique is implemented by feedback the output Q and QB to the MN3 and MN4 called as control transistors and input data D and DB is same as the output Q and QB prevents SET and RESET from being discharged. This results in flip-flop power saving at low data switching activities.

III. PROPOSED POWER GATED DIFFREENTIAL CONDITIONAL CAPTURING FLIP-FLOP

In this proposed power gated conditional capturing flip-flop uses coarse grain power gating technique. The schematic diagram of proposed flip-flop was shown in figure 2. By reducing the clock power and flip-flop power we can reduce the total power consumption. The LC Resonant based clock distribution network uses magnetic inductor which perform the operation of the variable inductor and LC tank should drive the entire clock network without any intermediate buffer to achieve maximum power saving in clock.

The second approach is to use conditional capturing flip-flop to eliminate redundant internal node transitions for minimizing flip-flop power at low data switching activities. The sinusoidal clock signal does not have any skew, delay problem and it is applied at the node of reduced swing inverters to reduce short circuit power and it is working efficiently in DCCFF.

In DCCFF MP1 and MP2 are charging transistors, MN1 and MN2 are clocking transistors, MN3 and MN4 are control transistors, MN5 and MN6 used for giving the input data, D and DB represents the input data, Q and QB represents the output. The clocking transistors are connected to the node X. The SET/RESET LATCH is used to latch the value created by the input signal and hold the value until the signal changes.

Power gating technique is used to reduce power consumption and it doesn’t supply current to blocks that are not in use. By reducing the transistor gate to source voltage power gating reduces leakage. In this method sleep transistors are coarsely placed.
Coarse-grained power gating is implemented in the DCCFF by connecting the sleep transistor between the permanent power supply and virtual power supply and it also controlling the Vdd supply. Q and QB is feedback to the control transistors which implements the capturing mechanism. The input data, output prevents SET and RESET from being discharged and the coarse-grained sleep transistors shares charging and discharging current. This results in the maximum power consumption.

IV. SIMULATION RESULTS AND PERFORMANCE COMPARISON.

The simulation results were obtained from TANNER and power consumption is calculated using MICROWIND in CMOS technology. The flip-flops were designed using the TSMC 0.18µm process technology at an operating temperature and supply voltage of 1.8V.

![Fig 3 Layout of power gated DCCFF](image3)

![Fig 4 proposed PG-DCCFF output waveform](image4)

The figure 3 shows the layout and figure 4 shows the output waveform. In figure 4 pink and green represents the D and DB (input data) Red represents the sinusoidal clock signal, blue and pink represents the Q and QB (output).

| TABLE 1 |
|-----------------|-----------------|-----------------|
| DESIGN          | DCCFF           | PG-DCCFF        |
| Total width (µm)| 40.9            | 45.7            |
| Total power (µm)| 16.942          | 12.045          |

*DCCFF-Differential Conditional Capturing Flip-Flop
**PG-DCCFF-Power gated Differential Conditional Capturing Flip-Flop

Table 1 represents the comparison between the DCCFF and PG-DCCFF. We analyze the different design in the views of total width and power consumption.

V. CONCLUSION
This paper presents the novel Differential Conditional capturing flip-flop using power gating to achieve low power and high performance application. The proposed flip-flop operates with a sinusoidal signal, because of this clock signal there is no skew and delay problem. To achieve power reduction by incorporating the power gating in the DCCFF and eliminates the unnecessary redundant transitions. By preventing the SET/RESET node from being discharged it results in flip-flop power saving.

REFERENCES