PIPELINED VEDIC MULTIPLIER

Dr.M.Ramkumar Raja¹, A.Anujaya², B.Bairavi³, B.Dhanalakshmi⁴, R.Dharani⁵
¹Associate Professor, ²,³,⁴,⁵Students
Department of Electronics and Communication Engineering
Coimbatore Institute of Engineering and Technology

ABSTRACT

Multipliers plays a vital role in various application like Arithmetic and logic unit, Digital processing and Accumulators. The drawbacks of using a Multipliers circuit is the delay in the circuit. Faster multipliers are designed to reduce the delay constraints. Vedic multiplier is known for it’s speed of operation. Among sixteen sutras in vedic multiplication techniques we are using “URDHVA TIRYAKBHYAM”. The Urdhva tiryakbhyam is the most efficient technique known for it’s speed of operation. Here we are aiming to construct the pipelined vedic multiplier using modelsim and Xilinx software.

KEYWORD

Vedicmultiplier, Urdhva tiryakbhyam

1. INTRODUCTION

Multiplier is the one which is largely used in the arithmetic and logic unit, digital processing and accumulators. Very huge number of adders are used for higher order multiplication. The vedic multiplication technique is based on the sixteen sutras and these technique are using the natural way of solving the higher order multiplication problems. Vedic multiplication technique are the fast one and requires less hardware. It is used to improve the computational speed of operation. Here we are implementing the pipelined 4*4 vedic multiplier using the urdhva tiryakbhyam among sixteen sutras to reduce the delay and to increase the throughput.

2. VEDIC METHOD

It is the method which is using the ancient technique. It is used to convert the complex multiplication into the simple one. It uses the natural method for implementing the higher order multiplications. The natural method uses the human mind work to reduce the complexity and implement the higher order multiplications. It is also having the effective algorithm for various complex application.

2.1 Technique used

Here we are using the \textit{vertical and crosswise technique}. The vedic multiplication technique is based on the urdhva tiryakbhyam. This technique is using the traditional method for multiplication of two decimal numbers. This technique is used to make the multiplication of higher order decimal numbers to be compatible in the digital hardware and to reduce the proceeding steps in the multiplication. It is the general multiplication technique and that can be used in all multiplications. The vertical and crosswise technique is used to obtain
the partial products by concurrent addition of these partial products inorder to reduce the steps.

This algorithm is generated for $n \times n$ bit numbers. The process is done in the parallel manner, the multiplier is independent of it’s clock frequency. Compared to the other multiplier it increases the delay and core area.

**Figure 1:**

**Question:** $42 \times 21 = ?$

**Step 1:**

- $4 \times 2 \quad \text{result} = 2$
- $2 \times 1 \quad \text{precarry} = 0$
- $82$

**Step 2:**

- $4 \times 2 \quad \text{result} = 8$
- $2 \times 1 \quad \text{precarry} = 0$
- $882$

**Step 3:**

- $4 \times 2 \quad \text{result} = 8$
- $2 \times 1 \quad \text{precarry} = 0$
- $882$

**Result:** $42 \times 21 = 882$

**Figure 1:** Multiplication of two decimal numbers $42 \times 21$

**VEDIC ARCHITECTURE**

The architecture of $2 \times 2$ vedic multiplier is shown below in the figure: 2.

This uses the ancient technique urdhva tiryakbhyam. The beauty of vedic multiplier is that can generate the partial products and additions are done concurrently.

For $2 \times 2$ Vedic multiplier:

- $a_0 = a_0 \times b_0$
- $a_1 \times 1 = a_1 \times b_0 + a_0 \times b_1$
- $a_2 \times 2 = a_1 + a_1 \times b_1$

For $4 \times 4$ vedic multiplier:

- $A = A_3A_2A_1A_0$ and $B = B_3B_2B_1B_0$

**Figure 3:** Structure for $4 \times 4$ bit vedic multiplication

Divide the no. of bits in the inputs equally in two parts. Let’s analysis $4 \times 4$ bit multiplication, say multiplicand $A = A_3A_2A_1A_0$ and
B=B3B2B1B0. Following are the output line for the multiplication result, S7S6S5S4S3S2S1S0. Let’s divide A and B into two parts, say “A3 A2” & “A1 A0” for A and “B3 B2” & “B1 B0” for B. To understand the concept, the block diagram of 4*4 bit vedic multiplier is shown in figure 4. To get final product S7S6S5S4S3S2S1S0 four, 2 bit vedic multiplier and three ripple carry adder are required. The ripple carry adder is constructed by cascading full adders blocks in series. It is composed of four full adders. The augend’s bits of a are added to the addend bits of b respectively of their binary position. Each bit addition creates a sum and a carry out. The carry out is then transmitted to the carry in of the next higher order bit. The final results creates a sum of four bits plus a carry out.

Figure: 4 Architecture of 4*4 vedic multiplier

IMPLEMENTATION & RESULTS

In this work, 4*4 bit vedic multiplier using “Urdhva Tiryakbhyam” sutra is implemented in the Verilog module. Logic synthesis and simulation was done using Xilinx ISE 12.1 and UK panel.

Table 1 Comparison of multiplier

<table>
<thead>
<tr>
<th>Bit</th>
<th>Array multiplier</th>
<th>Vedic multiplier(pipeline)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4*4 bits</td>
<td>31.003ns</td>
<td>13.110ns</td>
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</table>

For 4 bit piplined vedic multiplier it is observed that output of 1st data input is obtained after 4th clock cycle, after 5th clock cycle output of next data inputs and so on.

4*4 MULTIPLIER

4*4 VEDIC PIPELINED MULTIPLIER

CONCLUSION

Vedic multiplier is a proved to be more efficient one interms of speed of operation compare to conventional multipliers using Urdhva Tiryakbhyam sutra. This technique is suited for the application where the high speed multipliers are required. Hence it is used in the digital signal processing operations to increase the performance and speed.

REFERENCE


